Charge Pumps Shine in Portable Designs

New-generation ICs have combined with passive-component improvements to make charge-pump voltage conversion a favored approach in many applications. In many cases, the earlier charge pumps were considered either unsuitable or acceptable only with compromise. For example, an application that had relaxed accuracy, low load current, high noise tolerance, and minimal need for efficiency could benefit from a charge pump's lower cost, smaller size, simpler circuitry, and-of course-inductor-free operation.

Today's charge-pump ICs meet the demanding requirements of portable systems with improved precision, higher output current, output noise levels acceptable to sensitive RF applications, and battery life comparable to that of some inductor-based designs. The following discussion compares several IC charge-pump designs, presents "inductorless" power-supply applications, and offers guidelines for component selection.

A short primer

The term "charge pump " refers to a type of dc-dc voltage converter that uses capacitors rather than inductors or transformers to store and transfer energy. Charge pumps (often called switched-capacitor converters) include a switch or diode network that charges and discharges one or more capacitors. The most compelling advantage of a charge-pump circuit is the absence of inductors.

Why avoid inductors? Compared with capacitors, they have fewer purchasing sources, fewer standard specifications and dimensions, greater component height, more EMI, greater layout sensitivity, and higher cost. (Otherwise, they're great.) The newer generation of charge-pump ICs offers satisfactory operation even with the low-cost ceramic capacitors commonly used to bypass power supplies.

The basic charge pump can be implemented in an IC with analog switches, or in a discrete-component circuit with diodes (**Figure 1**). In the IC version, the switch network toggles between charge and discharge states, and in the discrete version, the clock waveform drives the charge and discharge states via diodes. In both cases the "flying capacitor " (C1) shuttles charge, and the "reservoir capacitor " (C2) holds charge and filters the output voltage. You can expand and modify this scheme as required to add regulation, reduce noise, obtain higher output voltage, etc.

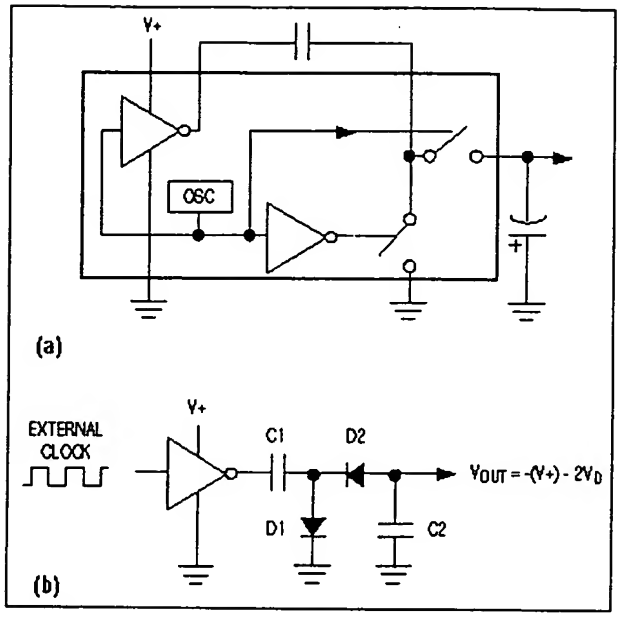


Figure 1. A basic charge pump provides voltage doubling or inversion. It can be implemented with on-chip switches (a) or discrete diodes (b).

Though charge pumps often serve as power sources for small circuit blocks or individual components such as interface ICs, they have not been widely used as system power supplies. This usage is changing, however: the output-current capability of charge pumps is increasing while the supply current required in portable designs is decreasing. In **Figure 2**, for example, the IC1 charge pump can generate 100mA at 3.3V when powered from a 2-cell battery of AA or AAA alkaline, NiCd, or NiMH cells, or a single primary lithium cell.

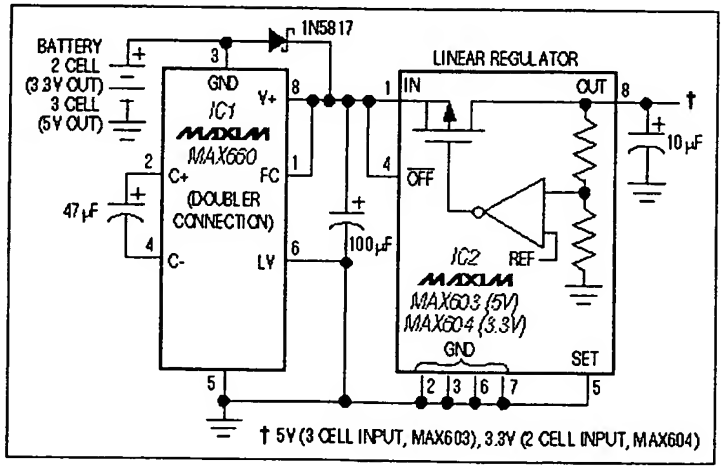


Figure 2. This charge-pump boost converter with linear regulator supplies 200mA at 3.3V with a 2-cell input, and 150mA at 5V with a 3-cell input.

The Figure 2 circuit can maintain its 3.3V output for inputs as low as 2.2V. For inputs ≥2.4V, it can supply short-term loads exceeding 200mA. For 5V systems with inputs as low as 3V, a similar design plus a 5V linear regulator supplies 150mA when powered from a 3-cell alkaline, NiCd, or NiMH battery, or one rechargeable lithium cell. The efficiency in both circuits varies from almost

80% (with low V_{IN}) to slightly more than 50% when the battery voltage is high (3.2V for two cells, or 4.8V for three cells).

Internally regulated charge pumps

The Figure 2 circuit overcomes the charge pump's lack of regulation by adding a regulator externally. Another option-if load currents are modest-is to add regulation on the chip. Regulation in a monolithic chip is generally accomplished either as linear regulation or as charge-pump modulation. Linear regulation offers the lowest output noise, and therefore provides better performance in (for example) a GaAsFET-bias circuit for RF amplifiers. Charge-pump modulation (which controls the switch resistance) offers more output current for a given die size (or cost), because the IC need not include a series pass transistor.

The circuit of **Figure 3** is useful both in main supplies and in backup supplies. It generates a regulated 5V output for load currents to 20mA and inputs ranging from 1.8V to 3.6V. For input voltages no lower than 3V, the output current can reach 50mA. The conversion efficiency (**Figure 4**) approaches that of an equivalent low-cost, inductor-based circuit. Note the variation with input voltage: efficiency exhibits a step change near V_{IN} = 3V, where the charge pump shifts automatically between its voltage-tripler and voltage-doubler modes of operation. For each "zone" of doubler or tripler operation, the highest efficiency occurs at the lowest V_{IN}. Within each zone, the efficiency declines as the losses increase with V_{IN}:

Power lost = I_{OUT} x [(2 or 3)V_{IN} - V_{OUT}]:

The Figure 3 circuit accomplishes regulation without a linear pass element, but its losses are the same as those of an unregulated doubler or tripler feeding into a linear regulator! This surprising result is a consequence of the unavoidable loss that occurs whenever the pump capacitors change voltage within a switching cycle. Consider two 1μF capacitors, one charged to 1V and one to 0V. Their total stored energy is:

$1/2CV^2 = 1/2(1\mu F)(1V^2) + 1/2(1\mu F)(0V^2) = 0.5\mu$Coulombs.

Connecting them in parallel recharges each to 0.5V, so the new total is:

$1/2(1\mu F)(0.5V^2) + 1/2(1\mu F)(0.5V^2) = 0.25\mu$Coulombs.

Thus, the energy lost in going from 1V to 0.5V (50%) is the same as that expected from a fixed-V_{OUT} doubler or tripler followed by a linear regulator. In Figure 3, efficiency is optimized by automatic shifts between doubler and tripler operation, which minimize the ΔV changes.

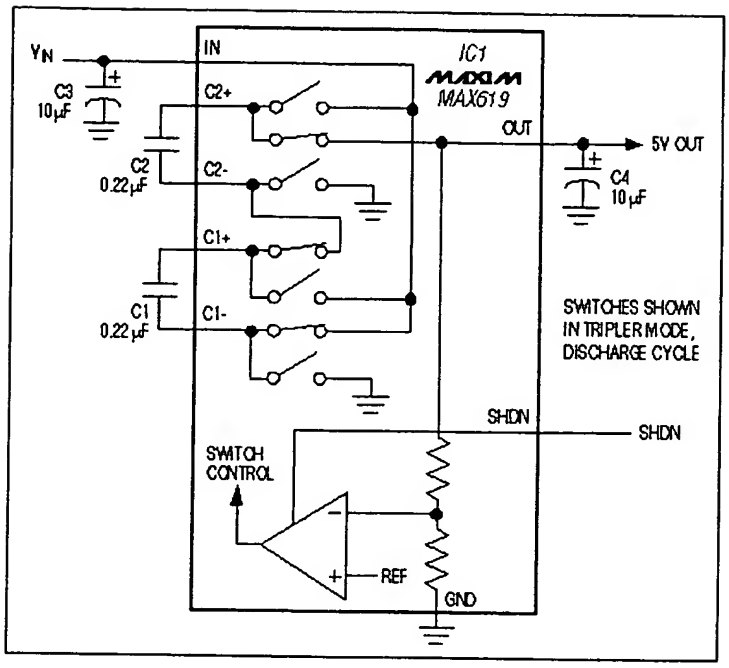


Figure 3. This IC contains a multi-switch boost converter with output regulation. The circuit either doubles or triples VIN to maximize efficiency. Switch-control information is fed back to maintain the output regulation.

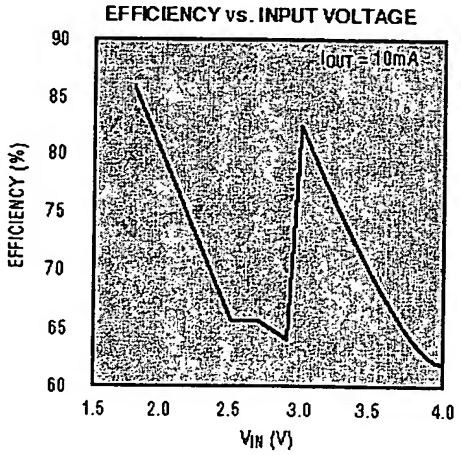


Figure 4. Discontinuities in the efficiency/VOUT profile for Figure 3 occur when the internal charge pump shifts between voltage doubling and tripling.

Operating current

Many capacitor-based voltage converters offer extremely low operating current-a useful feature in systems for which the load current is either uniformly low, or low most of the time. Thus, for smaller hand-held products the light-load operating currents can be much more important than full-load efficiency in determining battery life. In such products, the "off" state is not completely off, but rather a suspend or sleep state in which the supply current required (for µP and memory, for instance) may be 100µA or less. Battery life is affected directly if a comparable current is drawn by the power supply itself.

The supply current for a charge-pump IC is generally proportional to its operating frequency. You can minimize the current draw by running at the lowest possible frequency, but the penalty (for older charge-pump ICs) is higher ripple voltage, less IOUT capability, and the need for larger valued pump capacitors. Some ICs provide a pin-settable operating frequency to assist in making this tradeoff.

Newer charge-pump ICs employ another technique (on-demand switching), which enables low quiescent current and high-IOUT capability at the same time. Thus, the Figure 3 system incorporates on-demand circuitry that lowers the no-load supply current to 75µA (typical).

Although Figure 3's full-load efficiency (shown in Figure 4) is less than that found in most inductor-based designs, its very low operating current may allow a longer battery life. The effect of operating current on battery life depends on the fraction of operating time spent in the suspend or sleep state. The MAX619 in Figure 3, for instance, includes an on-demand oscillator that runs only when the output voltage falls below 5V. The resulting no-load quiescent current is only 75µA, and the device delivers output currents to 50mA using 0.22µA pump capacitors. Low operating current is also of interest when generating a backup voltage for lithium coin cells.

Flash memory

An application well suited for charge-pump conversion is the generation of a programming voltage for flash memory chips. The charge-pump approach provides a nearly ideal solution for credit-card-sized products in which the component height is severely restricted-particularly if it lowers the number of electrolytic capacitors or eliminates them altogether. An IC designed for this purpose (**Figure 5**) supplies a 12V "VPP" voltage suitable for programming 2-byte words of flash memory. Another IC (the MAX619, mentioned earlier) supplies a 5V VPP for 5V flash devices.

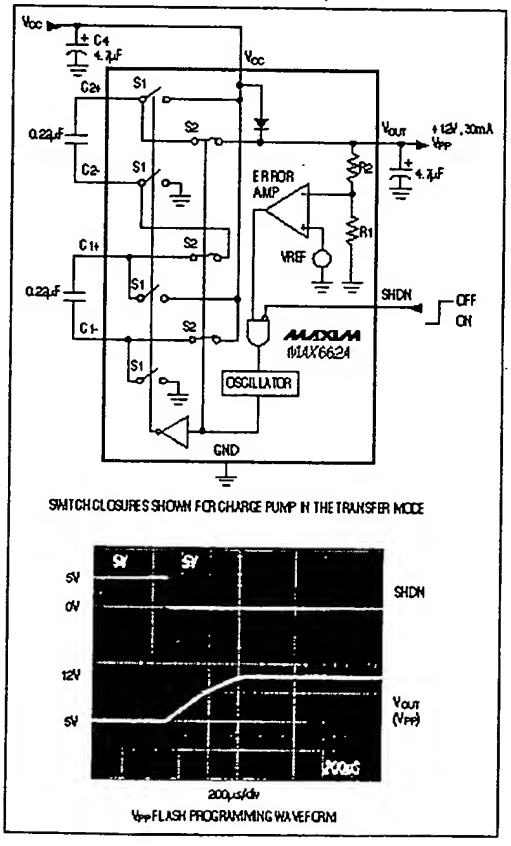


Figure 5. This IC generates the VPP programming voltage required for a 12V flash memory (12V). VOUT is fully regulated for loads of 30mA.

Compared with other types of voltage converters, the charge pump can provide superior performance in applications that process low-level signals or require low-noise operation. In some cases, the charge pump now allows voltage conversion in applications for which the only feasible solution had been a linear regulator. Note that these advantages don't apply to all charge pumps. When compared with inductor-based circuits, some disadvantages become apparent as well.

The most direct advantage is elimination of the magnetic fields and EMI that come with an inductor or transformer. One EMI source remains in a charge-pump circuit-the high charging current that flows to a "flying capacitor" when it connects to an input source or another capacitor with a different voltage. The instantaneous current flow is limited only by the associated capacitor ESR and switch resistance, which can be as low as 5Ω. Unless the charge pump is tailored for low-noise operation, the noise produced by these high-$\Delta I/\Delta t$ events can be eliminated only by post filtering or a large capacitance.

One example of a low-noise charge-pump converter is the MAX850 (**Figure 6**). Designed to generate very quiet negative bias voltages for GaAsFET RF power amplifiers, it combines an inverting charge pump with a low-noise, negative-output linear regulator. The MAX850 operates from 5VDC and has a high switching frequency (100kHz) that enables the use of small-valued external capacitors. An on-chip regulator lowers the output ripple and noise to only 2mVp-p. This noise (**Figure 7**) is remarkably low for a switching power supply.

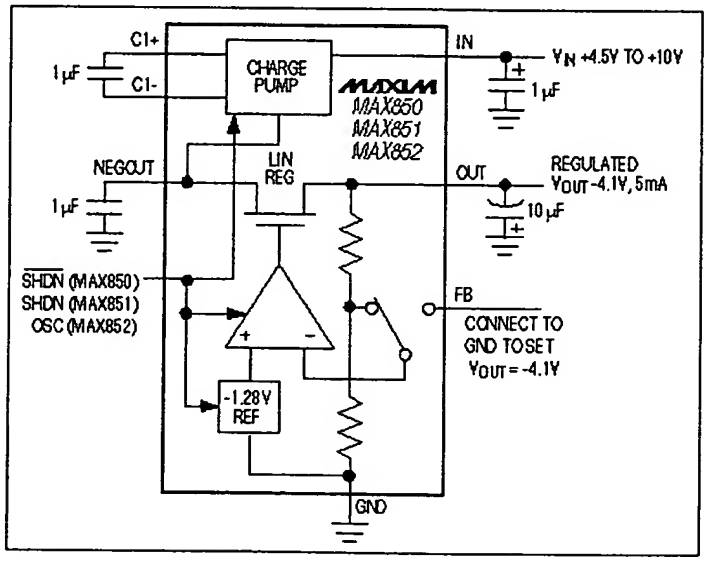


Figure 6. This GaAsFET-bias power supply contains a linear regulator that limits the output noise to 2mVp-p.

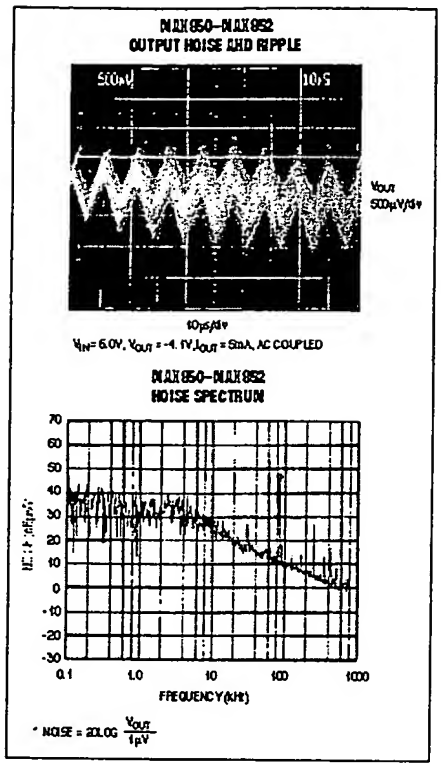


Figure 7. This noise plot for the Figure 6 circuit shows noise below 2mVp-p.

A similar approach taken in higher-current applications supplies a low-noise bias for the magneto-resistive read-write head in a high-capacity (2Gbytes and up) hard-disk drive. Such drives typically require -3V at 100mA, with no more than 10mVp-p of output noise and ripple. The pump output's switching transients again preclude a direct connection to the MR head preamp, but you can interpose a cheap yet serviceable linear regulator fashioned from three transistors (**Figure 8**). This arrangement is adequate for most uses. Its output accuracy, however, depends on the VIN tolerance because (for simplicity) VIN serves as a reference for the regulator. The output ripple and noise are about 5mVp-p.

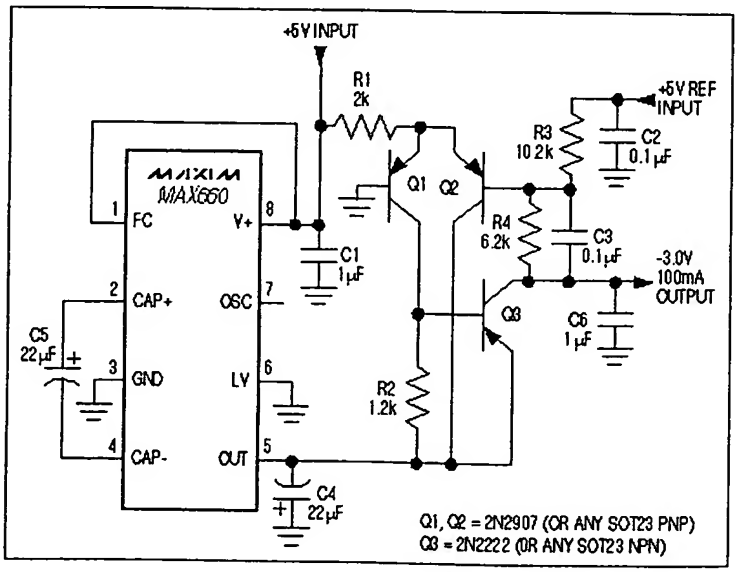


Figure 8. A cheap but serviceable three-transistor circuit adds a regulated 100mA, -3V output to a charge-pump IC.

Capacitor selection

A sometimes elusive bit of information relating to charge-pump designs is the minimum capacitor value needed for a particular load current. For most charge-pump ICs, the data sheet recommends only one or two capacitor values, yet (usually) the chip can operate with a wide range of values-especially when load currents are low. In most designs you should specify the smallest capacitor value that provides acceptable levels of output voltage, current, and ripple. These quantities depend on switching frequency and switch resistance as well as capacitance.

The effect of capacitance value on ripple and output current is illustrated by the eight graphs shown in **Figure 9** (and summarized in **Table 1**). Each graph includes five curves that supplement data-sheet information for three common charge-pump dc-dc converters from Maxim-the MAX660, MAX860, and MAX861:

1) MAX660, high-frequency mode (FC = V+), approximately 40kHz
2) MAX860, high-frequency mode (FC = OUT), approximately 100kHz
3) MAX860, medium-frequency mode (FC = GND), approximately 40kHz
4) MAX861, high-frequency mode (FC = OUT), approximately 200kHz
5) MAX861, medium-frequency mode (FC = GND), approximately 90kHz

These graphs show that lower load currents can often be supported by small ceramic capacitors. Evolving ceramic capacitor technology is producing higher values at lower costs, so you can now obtain ceramic capacitors to 10μF, at volume prices in the $0.30 range, from manufacturers such as United Chemicon (formerly Marcon), Tokin, TDK, and Murata Erie.

The frequency for each curve in Figure 9 is somewhat less than the typical found in the data sheet, because V_{IN} is specified on the low side: 4.5V = 5V - 10%, and 3.0V = 3.3V - 10%. Some of the graphs depict higher current at 2.0μF than at 2.2μF. That occurs because the 1μF and 2μF values are ceramic chips (with Z5U dielectric), and the values from 2.2μF up are tantalum types (AVX TPS series). Current and ripple data was collected by loading the outputs until V_{OUT} reached the value shown in Table 1. (Ripple improvement is negligible at higher values of capacitance.) V_{OUT} is higher at lower load currents, but -(V_{OUT}) never exceeds V_{IN}.

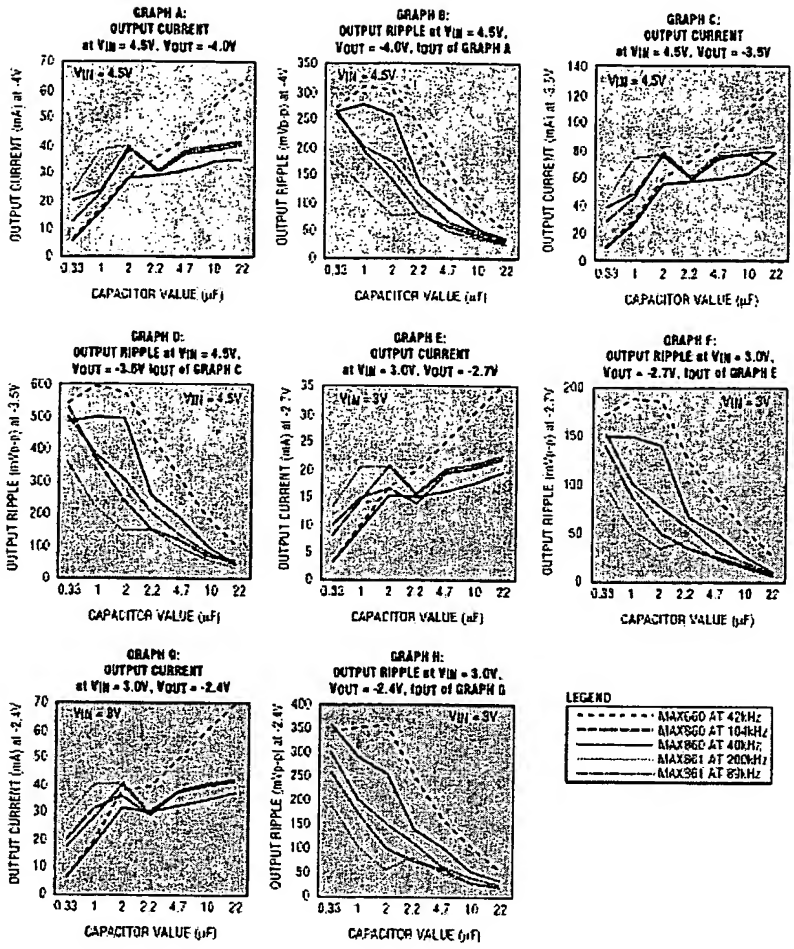


Figure 9. These graphs (A-H) show the relationships among operating frequency, capacitance value, operating current, and output voltage for a charge-pump voltage converter. For a given load, the data enables selection of the minimum capacitance value and operating current.

Table 1. Summary of graphs in Figure 9

GRAPH	V_{IN} (V)	V_{OUT} (V)	PLOTTED DATA
A	4.5	-4.0	I_{OUT} vs. cap. value (0.33µF to 22µF)
B	4.5	-4.0	Ripple vs. cap. value, at I_{OUT} from "A"
C	4.5	-3.5	I_{OUT} vs. cap. value
D	4.5	-3.5	Ripple vs. cap. value, at I_{OUT} from "C"

GRAPH	V_{IN} (V)	V_{OUT} (V)	PLOTTED DATA
E	3.0	-2.7	I_{OUT} vs. cap. value
F	3.0	-2.4	Ripple vs. cap. value, at I_{OUT} from "E"
G	3.0	-2.4	I_{OUT} vs. cap. value
H	3.0	-2.7	Ripple vs. cap. value, at I_{OUT} from "G"

Charge-pump tricks

Power conversion by integrated charge pumps is, of course, predated by the use of discrete capacitors for that purpose. Charge-pump techniques have been used in 50Hz/60Hz ac-line supplies for many years, and also in high-voltage multipliers to achieve outputs of several kV. The use of CMOS analog switches has enabled the integration of complex functions with very few parts. As another advantage, CMOS switches exhibit a virtual zero drop at low current, versus the

minimum 0.6V drop across a diode switch. But, in some cases, the addition of discrete components can add performance, even in applications employing the latest charge-pump ICs.

A low-power converter of 5V to ±20V can be made surprisingly small by enhancing a dual-output charge-pump IC with an extra boost stage composed of discrete diodes. Such supplies are useful for CCD power supplies, LCD bias, and varactor tuners. The MAX864 on its own can generate ±10V (minus load-proportional losses) from a 5V input, or ±6.6V from a 3.3V input. Using additional diode-capacitor stages (**Figure 10**), these outputs can be doubled again to approximately ±4VIN, or multiplied by 1.5 to approximately ±3VIN. Note that the external diode/capacitor network connects to C1 for ±15V outputs, or to C2 for ±20V outputs.

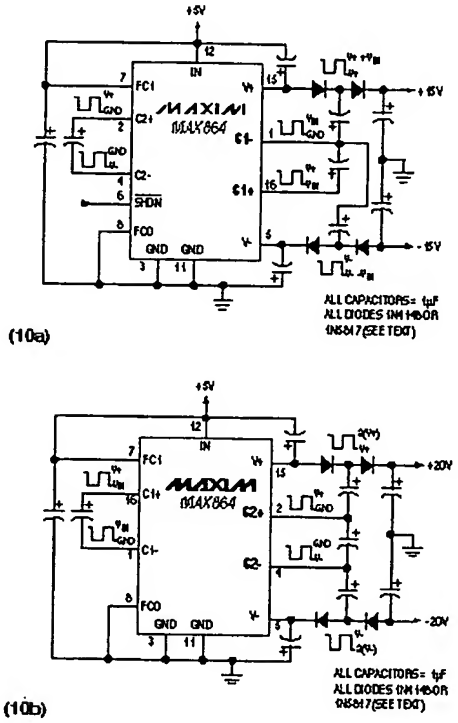


Figure 10. You can obtain higher output voltage from many charge-pump ICs by augmenting the circuit with external diodes and capacitors. These circuits supply up to ±20V.

Figure 11 illustrates the output voltage versus load current for each circuit in Figure 10, using both silicon diodes (for lowest cost) and Schottky diodes (for highest output). These circuits can supply as much as 20mA, and the 1µF filter capacitors yield less than 100mV of output ripple. If desired, you can lower that level considerably with slightly larger capacitors. The ICs in Figure 10 are set for 100kHz operation to allow use of 1µF capacitors, which results in a no-load supply current of 7mA. You can pin-program a lower frequency that lowers the supply current to 600µA, but to achieve the output currents shown in Figure 11 you'll need larger capacitors of 10µF.

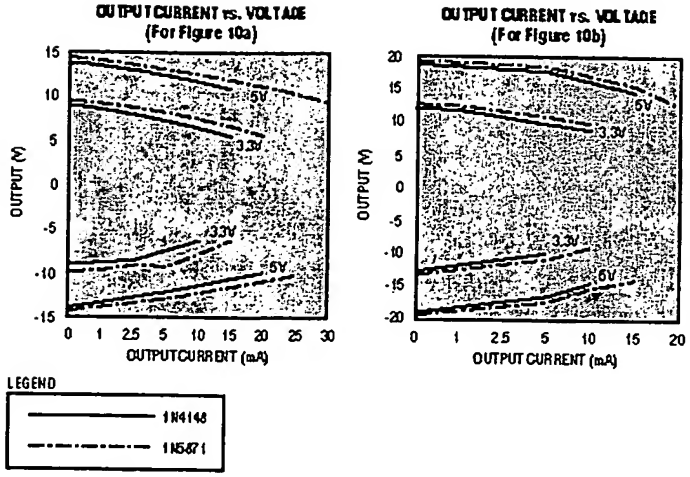


Figure 11. These graphs show VOUT vs. IOUT for the two circuits of Figure 10.

Normally, a single-stage charge-pump converter cannot generate negative outputs greater than its positive input voltage. To achieve negative outputs of -8V or more from inputs of 2.5V to 5.5V, add discrete diodes as shown in **Figure 12**. Peak-to-peak noise is the same as shown in Figure 7, and the available output current for a given regulated output voltage is shown at five discrete input voltages in **Figure 13**.

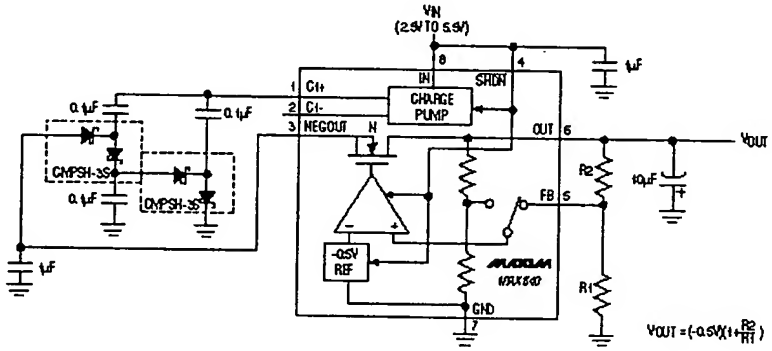


Figure 12. The diode-capacitor network external to this low-noise regulated charge pump lowers the minimum input voltage from 4.5V to 2.5V.

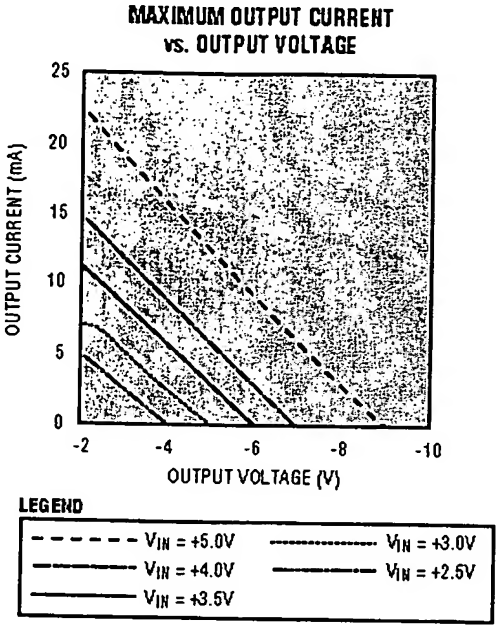


Figure 13. These curves show IOUT vs. regulated VOUT for the Figure 12 circuit.

To avoid the need to supply battery or line voltage to low-power computer peripherals, you can siphon off a few milliwatts from the serial port. The common PC mouse and other such designs rely on the modem control signals DTR and RTS, but the circuit of **Figure 14** gets power from the TX line of a 3-wire port. Its output capability (8mA) is sufficient for a CMOS microcontroller and some support electronics. The TX line idles at a negative voltage, so the IC's normal input polarity is reversed (the negative input voltage applied between the OUT pin and ground enables the IC to pump backward from its normal direction). Zener diode D1 provides shunt regulation for a 4.7V output.

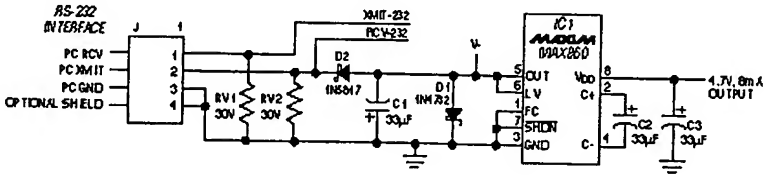


Figure 14. Operating in a voltage-doubler mode, this charge pump converts a negative input voltage (from the TX line of an RS-232 port) to a semi-regulated 5V output at 8mA.

Charge-pump ICs can help shrink the power supply in a portable system, so it pays to monitor the new technologies and new IC designs constantly being introduced by manufacturers. Maxim, for instance, offers a variety of charge-pump ICs, listed in **Tables 2-4**.

Table 2. Single-output charge pumps

PARAMETER	MAX828	MAX829	MAX860	MAX861	MAX660	MAX1044	ICL7662	ICL7660
PACKAGE	SOT23-5	SOT23-5	SO-8, µMAX	SO-8, µMAX	SO-8	SO-8	SO-8	SO-8, µMAX
OUTPUT CURRENT (mA typ)	0.02	0.15	0.2 @ 6kHz, 0.6 @ 50kHz, 1.4 @ 130kHz	0.3 @ 12kHz, 1.1 @ 100kHz, 2.5 @ 250kHz	0.12 @ 5kHz, 1 @ 40kHz	0.03	0.25	0.02
OUTPUT (Ω typ)	20	20	12	12	6.5	35	125	55
PUMP RATE (kHz)	12	35	6, 50, 130	12, 100, 150	5, 40	5	10	10
INPUT (V)	1.25 to 5.5	1.25 to 5.5	1.5 to 5.5	1.5 to 5.5	1.5 to 5.5	1.5 to 10	1.5 to 20	1.5 to 10

Table 3. Regulated charge pumps

PARAMETER	MAX619	MAX662A	MAX840/843/844	MAX850/1/2/3
PACKAGE	SO-8	SO-8	SO-8	SO-8
OUTPUT CURRENT (mA typ)	0.035	0.125	0.75	2
OUTPUT (V)	5 ±4%	12 ±5%	-2.5 or set -0.5 to -9.4	-4.1 or set -0.5 to -9
GUARANTEED Iout (mA)	50	30	4	5
PUMP RATE (kHz)	500	500	100 ±20	100 ±20
INPUT (V)	2.0 to 3.6	4.5 to 5.5	2.5 to 10	4.5 to 10
SHUTDOWN	Yes	Yes	Yes	Yes
FEATURES/COMMENTS	—	Flash memory Vpp	Low-noise GaAsFET bias	Low-noise GaAsFET bias

Table 4. Multi-output charge pumps

PARAMETER	MAX680	MAX855	MAX864
PACKAGE	SO-8	µMAX	QSOP
OUTPUT CURRENT (mA typ)	1	0.6	0.6 @ 7MHz, 2.4 @ 33MHz, 7.0 @ 90MHz, 12 @ 185MHz
OUTPUT (V)	±10V (5V in)	±10V (5V in)	±10V (5V in)
POSITIVE Zout (Ω typ)	150	150	55
NEGATIVE Zout (Ω typ)	50	75	34
PUMP RATE (kHz)	8	24	7, 33, 100, 185
INPUT (V)	2 to 5	2 to 5	1.75 to 6
SHUTDOWN	No	No	Yes

features

- Regulated 3.3-V Output Voltage With up to 100-mA Output Current From a 1.8-V to 3.6-V Input Voltage
- Less Than 5-$mV_{(PP)}$ Output Voltage Ripple Achieved With Push-Pull Topology
- Integrated Low-Battery and Power-Good Detector
- Switching Frequency Can Be Synchronized to External Clock Signal
- Extends Battery Usage With up to 90% Efficiency and 35-μA Quiescent Supply Current
- Easy-to-Design, Low Cost, Low EMI Power Supply Since No Inductors Are Used
- 0.05-μA Shutdown Current, Battery is Isolated From Load in Shutdown Mode
- Compact Converter Solution in UltraSmall 10-pin MSOP With Only Four External Capacitors Required
- Evaluation Module Available (TPS60200EVM-145)

applications

- Replaces DC/DC Converters With Inductors in Battery Powered Applications Like:
  - Two Battery Cells to 3.3-V Conversion
  - MP3 Portable Audio Players
  - Battery-Powered Microprocessor Systems
  - Backup-Battery Boost Converters
  - PDA's, Organizers, and Cordless Phones
  - Handheld Instrumentation
  - Glucose Meters and Other Medical Instruments

description

The TPS6020x step-up, regulated charge pumps generate a 3.3-V ±4% output voltage from a 1.8-V to 3.6-V input voltage. The devices are typically powered by two Alkaline, NiCd, or NiMH battery cells and operate down to a minimum supply voltage of 1.6 V. Continuous output current is a minimum of 100 mA from a 2-V input. Only four external capacitors are needed to build a complete low-ripple dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple, as current is continuously transferred to the output.

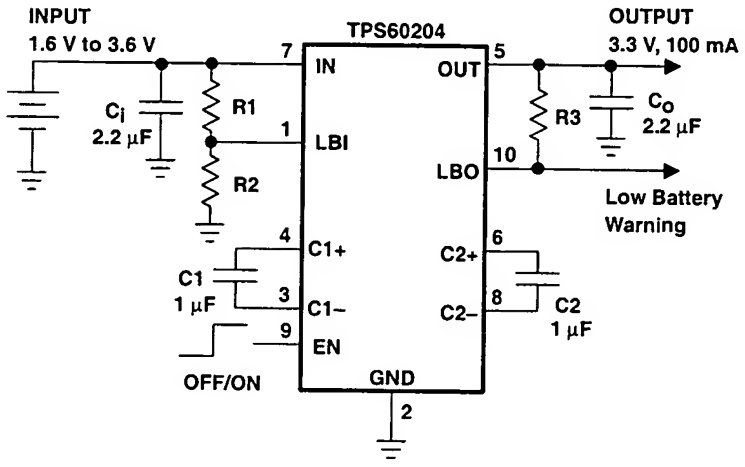
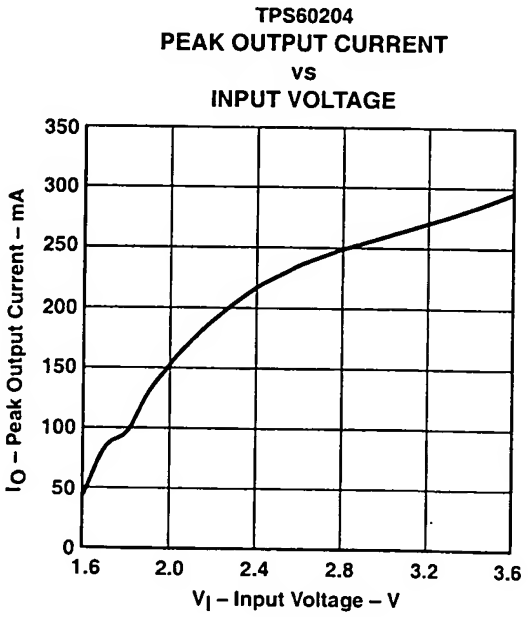


Figure 1. Typical Application Circuit With Low-Battery Warning



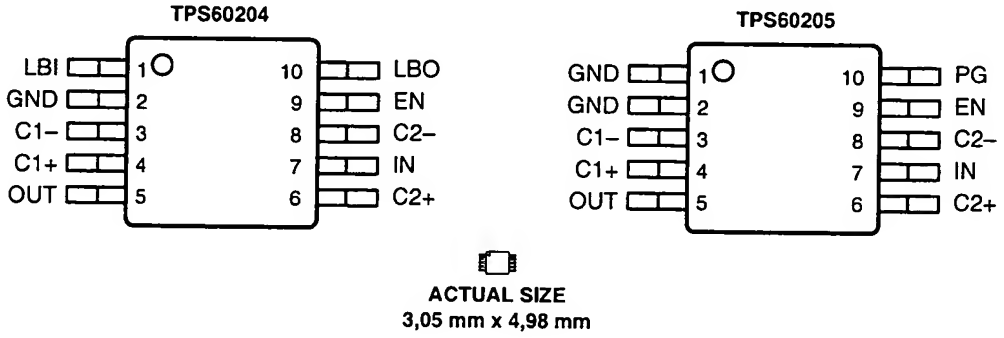
description (continued)

The devices operate in the newly developed LinSkip mode. In this operating mode, the device switches seamlessly from the power saving pulse-skip mode at light loads to the low-noise constant-frequency, linear-regulation mode once the output current exceeds the LinSkip threshold of about 7 mA. Even in pulse-skip mode, the output ripple is maintained at a very low level because the output resistance of the charge pump is still regulated.

Three operating modes can be programmed using the EN pin. EN = low disables the device, shuts down all internal circuits, and disconnects the output from the input. EN = high enables the device and programs it to run from the internal oscillator. The devices operate synchronized to an external clock signal if EN is clocked; thus, switching harmonics can be controlled and minimized. The devices include a low-battery detector that issues a warning if the battery voltage drops below a user-defined threshold voltage, or a power-good detector that goes active when the output voltage reaches about 90% of its nominal value.

Device options with either a low-battery or power good detector are available. This dc/dc converter requires no inductors, therefore, EMI of the system is reduced to a minimum. It is available in the small 10-pin MSOP package (DGS).

DGS PACKAGES



ACTUAL SIZE
3,05 mm x 4,98 mm

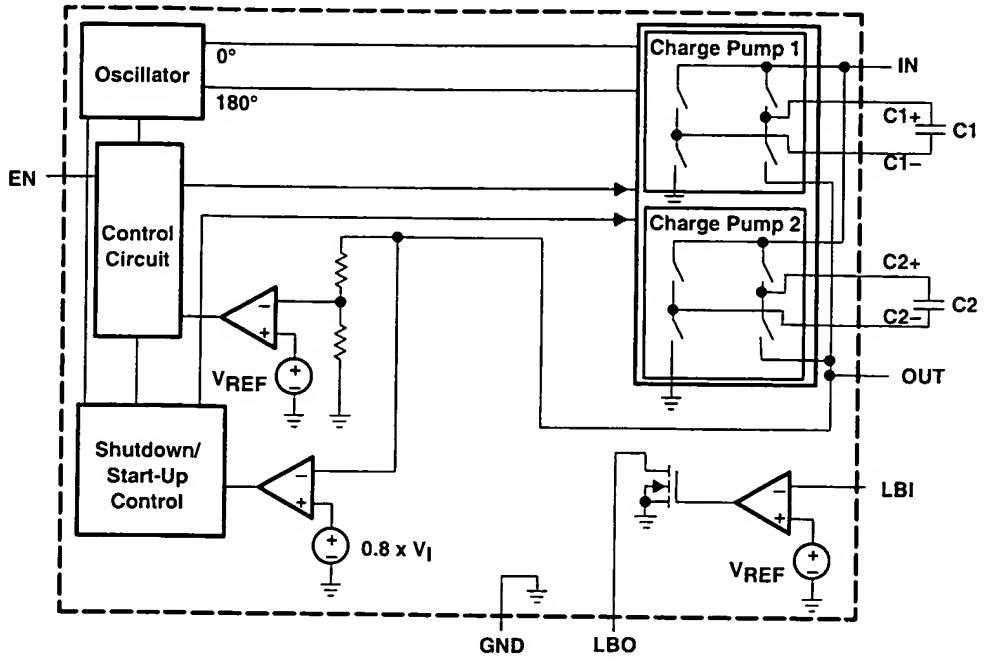
AVAILABLE OPTIONS

T_A	PART NUMBER†	MARKING DGS PACKAGE	OUTPUT CURRENT (mA)	OUTPUT VOLTAGE (V)	DEVICE FEATURES
–40°C to 85°C	TPS60204DGS	AFB	100	3.3	Low-battery detector
	TPS60205DGS	AFC	100	3.3	Power-good detector

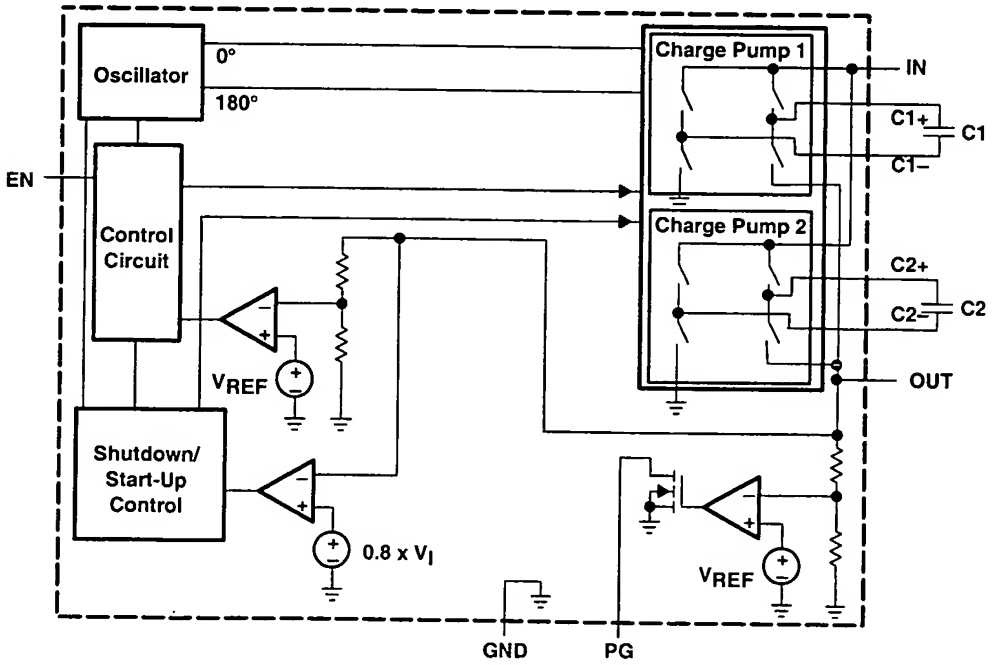
† The DGS package is available taped and reeled. Add R suffix to device type (e.g., TPS60204DGSR) to order quantities of 2500 devices per reel.

functional block diagrams

TPS60204 with low-battery detector



TPS60205 with power-good detector



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
C1+	4		Positive terminal of the flying capacitor C1
C1–	3		Negative terminal of the flying capacitor C1
C2+	6		Positive terminal of the flying capacitor C2
C2–	8		Negative terminal of the flying capacitor C2
EN	9	I	Device-enable input. Three operating modes can be programmed with the EN pin. – EN = Low disables the device. Output and input are isolated in the shutdown. – EN = High lets the device run from the internal oscillator. – If an external clock signal is applied to the EN pin, the device is in syncmode and runs synchronized at the frequency of the external clock signal.
GND	2		Ground
IN	7	I	Supply input. Bypass IN to GND with a capacitor of the same size as C_O.
LBI/GND	1	I	Low-battery detector input for the TPS60204. A low-battery warning is generated at the LBO pin when the voltage on LBI drops below the threshold of 1.18 V. Connect LBI to GND if the low-battery detector function is not used. For the TPS60205, this pin has to be connected to ground (GND pin).
LBO/PG	10	O	Open-drain low-battery detector output for the TPS60204. This pin is pulled low if the voltage on LBI drops below the threshold of 1.18 V. A pullup resistor should be connected between LBO and OUT or any other logic supply rail that is lower than 3.6 V. Open-drain power-good detector output for the TPS60205. As soon as the voltage on OUT reaches about 90% of it is nominal value this pin goes active high. A pullup resistor should be connected between PG and OUT or any other logic supply rail that is lower than 3.6 V.
OUT	5	O	Regulated 3.3-V power output. Bypass OUT to GND with the output filter capacitor C_O.

detailed description

operating principle

The TPS6020x charge pumps provide a regulated 3.3-V output from a 1.8-V to 3.6-V input. They deliver up to 100-mA load current while maintaining the output at 3.3 V ±4%. Designed specifically for space critical battery powered applications, the complete converter requires only four external capacitors. The device is using the push-pull topology to achieve lowest output voltage ripple. The converter is also optimized for smallest board space. It makes use of small sized capacitors, with the highest output current rating per output capacitance and package size.

The TPS6020x circuits consist of an oscillator, a 1.18-V voltage reference, an internal resistive feedback circuit, an error amplifier, two charge pump power stages with high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (see functional block diagrams).

push-pull operating mode

The two single-ended charge pump power stages operate in the so-called push-pull operating mode, i.e., they operate with a 180°C phase shift. Each single-ended charge pump transfers charge into its transfer capacitor (C1 or C2) in one half of the period. During the other half of the period (transfer phase), the transfer capacitor is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation assures an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name voltage doubler). In order to provide a regulated fixed output voltage of 3.3 V, the TPS6020x devices use either pulse-skip or constant-frequency linear-regulation control mode. The mode is automatically selected based on the output current. If the load current is below the LinSkip current threshold, it switches into the power-saving pulse-skip mode to boost efficiency at low output power.

detailed description (continued)

constant-frequency mode

When the output current is higher then the LinSkip current threshold, the charge pump runs continuously at the switching frequency $f_{(OSC)}$. The control circuit, fed from the error amplifier, controls the charge on C1 and C2 by controlling the gates and hence the $r_{DS(ON)}$ of the integrated MOSFETs. When the output voltage decreases, the gate drive increases, resulting in a larger voltage across C1 and C2. This regulation scheme minimizes output ripple. Since the device switches continuously, the output signal contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads. For this reason, the device switches seamlessly into the pulse-skip mode when the output current drops below the LinSkip current threshold.

pulse-skip mode

The regulator enters the pulse-skip mode when the output current is lower than the LinSkip current threshold of 7 mA. In the pulse-skip mode, the error amplifier disables switching of the power stages when it detects an output voltage higher than 3.3 V. The controller skips switching cycles until the output voltage drops below 3.3 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. A 30-mV output voltage offset is introduced in this mode.

The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except the voltage reference and error amplifier when the output is higher than 3.3 V. Even in pulse-skip mode the $r_{DS(ON)}$ of the MOSFETs is controlled. This way the energy per switching cycle that is transferred by the charge pump from the input to the output is limited to the minimum that is necessary to sustain a regulated output voltage, with the benefit that the output ripple is kept to a minimum. When switching is disabled from the error amplifier, the load is also isolated from the input.

start up and shutdown

During start-up, i.e. when EN is set from logic low to logic high, the output capacitor is directly connected to IN and charged up with a limited current until the output voltage V_O reaches $0.8 \times V_I$. When the start-up comparator detects this limit, the converter begins switching. This precharging of the output capacitor guarantees a short start-up time. In addition, the inrush current into an empty output capacitor is limited. The converter can start into a full load, which is defined by a 33-Ω or 66-Ω resistor, respectively.

Driving EN low disables the converter. This disables all internal circuits and reduces the supply current to only 0.05 µA. The device exits shutdown once EN is set high. When the device is disabled, the load is isolated from the input. This is an important feature in battery operated products because it extends the products shelf life.

synchronization to an external clock signal

The operating frequency of the charge pump is limited to 400 kHz in order to avoid interference in the sensitive 455-kHz IF band. The device can either run from the integrated oscillator, or an external clock signal can be used to drive the charge pump. The maximum frequency of the external clock signal is 800 kHz. The switching frequency used internally to drive the charge pump power stages is half of the external clock frequency. The external clock signal is applied to the EN pin. The device will switch off if the signal on EN is hold low for more than 10 µs.

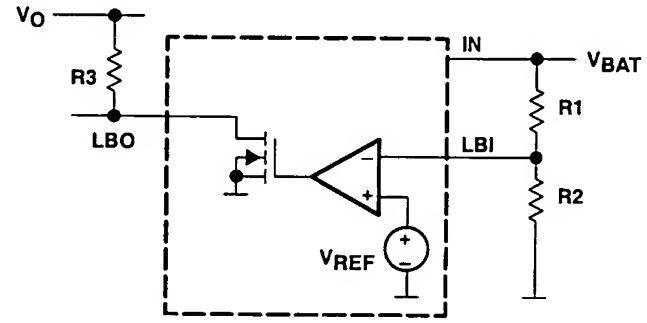
When the load current drops below the LinSkip current threshold, the devices will enter the pulse-skip mode but stay synchronized to the external clock signal.

detailed description (continued)

low-battery detector (TPS60204)

The low-battery comparator trips at 1.18 V ±4% when the voltage on pin LBI ramps down. The voltage $V_{(TRIP)}$ at which the low-battery warning is issued can be adjusted with a resistive divider as shown in Figure 2. The sum of resistors R1 and R2 is recommended to be in the 100-kΩ to 1-MΩ range. When choosing R1 and R2, be aware of the input leakage current into the LBI pin.

LBO is an open drain output. An external pullup resistor to OUT, or any other voltage rail in the appropriate range, in the 100-kΩ to 1-MΩ range is recommended. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected. The low-battery detector is disabled when the device is switched off.



$$V_{(TRIP)} = 1.18\ V \left(1 + \frac{R1}{R2}\right)$$

Figure 2. Programming of the Low-Battery Comparator Trip Voltage

A 100-nF ceramic capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

Formulas to calculate the resistive divider for low-battery detection, with V_{LBI} = 1.13 V to 1.23 V and the sum of resistors R1 and R2 equal 1 MΩ:

$$R2 = 1\ M\Omega \times \frac{V_{LBI}}{V_{Bat}} \quad (1)$$

$$R1 = 1\ M\Omega - R2 \quad (2)$$

Formulas to calculate the minimum and maximum battery voltage:

$$V_{Bat(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}} \quad (3)$$

$$V_{Bat(max)} = V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}} \quad (4)$$

detailed description (continued)

Table 1. Recommended Values for the Resistive Divider From the E96 Series (±1%)

V_{IN}/V	R1/kΩ	R2/kΩ	$V_{TRIP(MIN)}$/V	$V_{TRIP(MAX)}$/V
1.6	267	750	1.524	1.677
1.7	301	681	1.620	1.785
1.8	340	649	1.710	1.887
1.9	374	619	1.799	1.988
2.0	402	576	1.903	2.106

power-good detector (TPS60205)

The power-good output is an open-drain output that pulls low when the output is out of regulation. When the output rises to within 90% of its nominal voltage, the power-good output is released. Power-good is high impedance in shutdown. In normal operation, an external pullup resistor must be connected between PG and OUT, or any other voltage rail in the appropriate range. The resistor should be in the 100-kΩ to 1-MΩ range. If the PG output is not used, it should remain unconnected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range: IN, OUT, EN, LBI, LBO, PG to GND ..... –0.3 V to 3.6 V
C1+, C2+ to GND ..... –0.3 V to (V_O + 0.3 V)
C1–, C2– to GND ..... –0.3 V to (V_I + 0.3 V)
Continuous total power dissipation ..... See dissipation rating table
Continuous output current TPS60204, TPS60205 ..... 150 mA
Storage temperature range, T_{stg} ..... –55°C to 150°C
Maximum junction temperature, T_J ..... 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGS	424 mW	3.4 mW/°C	187 mW	136 mW

The thermal resistance junction to ambient of the DGS package is R_{TH-JA} = 294°C/W.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage range, V_I	1.6		3.6	V
Input capacitor, C_i		2.2		µF
Flying capacitors, C1, C2		1		µF
Output capacitor, C_O		2.2		µF
Operating junction temperature, T_J	–40		125	°C

electrical characteristics at C_i = 2.2 µF, C1 = C2 = 1 µF, C_O = 2.2 µF, T_A = –40°C to 85°C, V_I = 2.4 V, EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O(MAX)}$	Maximum continuous output current	V_I = 2 V	100			mA
V_O	Output voltage	1.6 V < V_I < 1.8 V, 0 < I_O < 0.25 × $I_{O(MAX)}$	3			V
		1.8 V < V_I < 2 V, 0 < I_O < 0.5 × $I_{O(MAX)}$	3.17		3.43	
		2 V < V_I < 3.3 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.43	
		3.3 V < V_I < 3.6 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.47	
V_{PP}	Output voltage ripple	I_O = $I_{O(MAX)}$		5		mV_{PP}
$I_{(Q)}$	Quiescent current (no-load input current)	I_O = 0 mA, V_I = 1.8 V to 3.6 V		35	70	µA
$I_{(SD)}$	Shutdown supply current	EN = 0 V		0.05	1	
$f_{(OSC)}$	Internal switching frequency		200	300	400	kHz
$f_{(SYNC)}$	External clock signal frequency		400	600	800	
	External clock signal duty cycle		30%		70%	
V_{IL}	EN input low voltage	V_I = 1.6 V to 3.6 V			0.3 × V_I	V
V_{IH}	EN input high voltage	V_I = 1.6 V to 3.6 V	0.7 × V_I			
$I_{lkg(EN)}$	EN input leakage current	EN = 0 V or V_I		0.01	0.1	µA
	Output capacitor auto discharge time	EN is set from V_I to GND, Time until V_O < 0.5 V		0.6		ms
	Output leakage current in shutdown	EN = 0 V, T_A = –40 to 85°C			5	µA
		EN = 0 V, T_A ≤ 65°C			3	
	LinSkip threshold	V_I = 2.2 V		7		mA
	Output load regulation	10 mA < I_O < $I_{O(MAX)}$; T_A = 25°C		0.01		%/mA
	Output line regulation	2 V < V_I < 3.3 V, I_O = 0.5 x $I_{O(MAX)}$, T_A = 25°C		0.6		%/V
$I_{(SC)}$	Short circuit current	V_I = 2.4 V, V_O = 0 V		60		mA

electrical characteristics for low-battery comparator of devices TPS60204 at T_A = –40°C to 85°C, V_I = 2.4 V and EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(LBI)}$	LBI trip voltage	V_I = 1.6 V to 2.2 V, T_C = 0°C to 70°C	1.13	1.18	1.23	V
	LBI trip voltage hysteresis	For rising voltage at LBI		10		mV
$I_{I(LBI)}$	LBI input current	$V_{(LBI)}$ = 1.3 V		2	50	nA
$V_{O(LBO)}$	LBO output voltage low	$V_{(LBI)}$ = 0 V, $I_{(LBO)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO leakage current	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 3.3 V		0.01	0.1	µA

NOTE: During start-up of the converter the LBO output signal is invalid for the first 500 µs.

electrical characteristics for power-good comparator of devices TPS60205 at T_A = –40°C to 85°C, V_I = 2.4 V and EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PG)}$	Power-good trip voltage	T_C = 0°C to 70°C	0.87 × V_O	0.91 × V_O	0.95 × V_O	V
$V_{hys(PG)}$	Power-good trip voltage hysteresis	V_O decreasing, T_C = 0°C to 70°C		1%		
$V_{O(PG)}$	Power-good output voltage Low	V_O = 0 V, $I_{(PG)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	V_O = 3.3 V, $V_{(PG)}$ = 3.3 V		0.01	0.1	µA

NOTE: During start-up of the converter the PG output signal is invalid for the first 500 µs.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURES
η	Efficiency	vs Output current (TPS60204, TPS60205)	3
		vs Input voltage	4
I_Q	Quiescent supply current	vs Input voltage	5
V_O	Output voltage	vs Output current	6
		vs Input voltage	7
V_O	Output voltage ripple	vs Time	8, 9, 10
	Start-up timing		11
	Load transient response		12, 13
I_O	Peak output current	vs Input voltage	14

NOTE: All typical characteristics were measured using the typical application circuit of Figure 14 (unless otherwise noted).

TPS60204, TPS60205
EFFICIENCY
vs
OUTPUT CURRENT

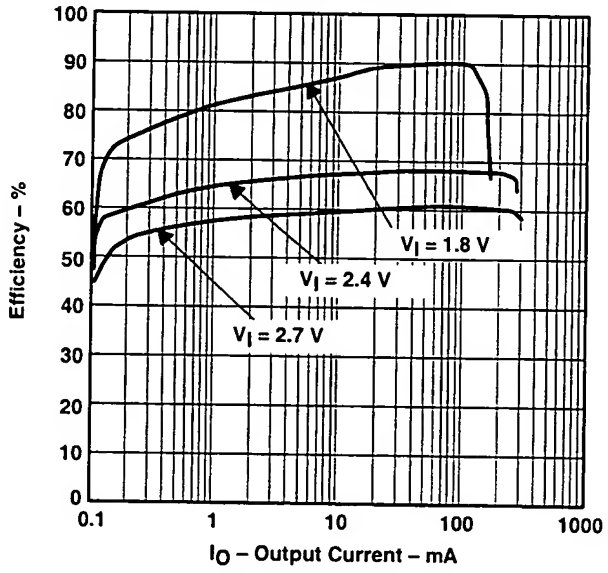


Figure 3

EFFICIENCY
vs
INPUT VOLTAGE

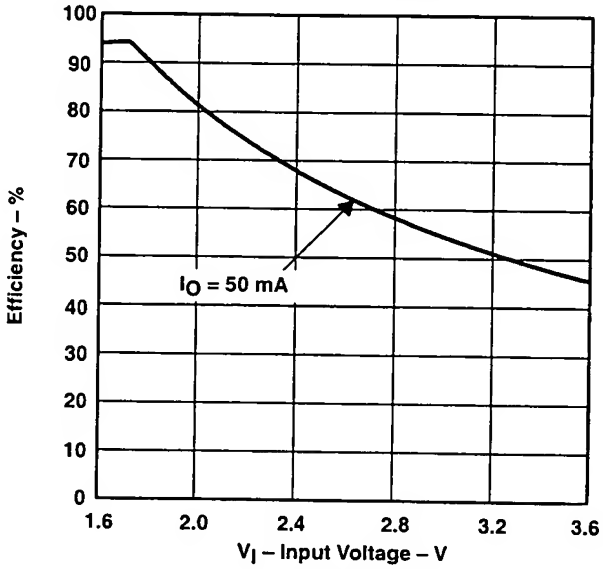


Figure 4

TYPICAL CHARACTERISTICS

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

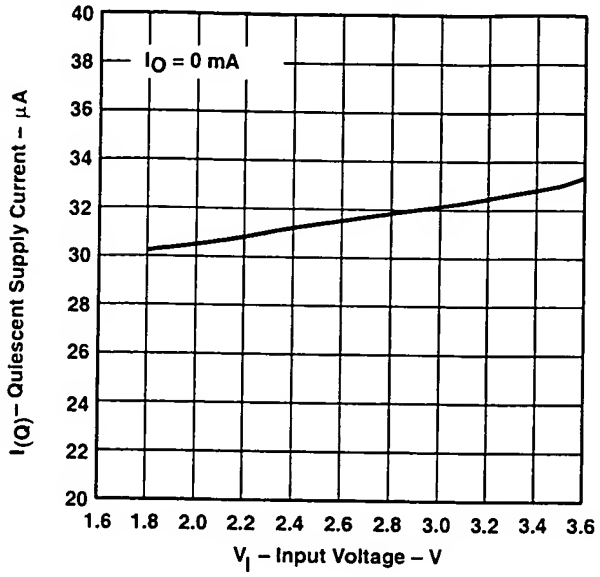


Figure 5

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

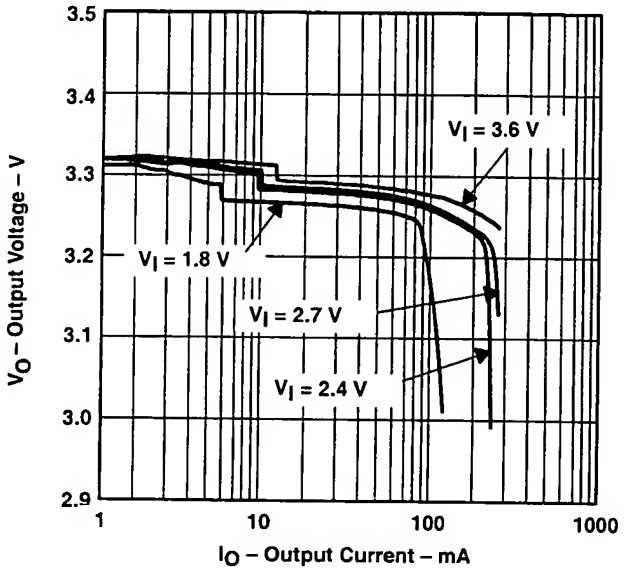


Figure 6

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

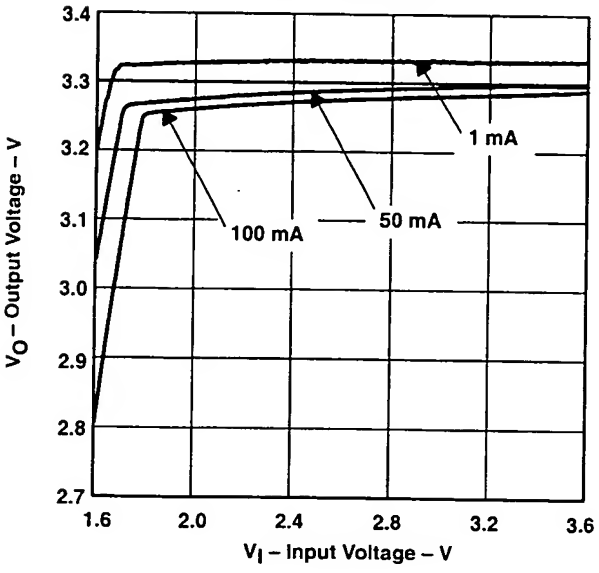


Figure 7

OUTPUT VOLTAGE RIPPLE
vs
TIME

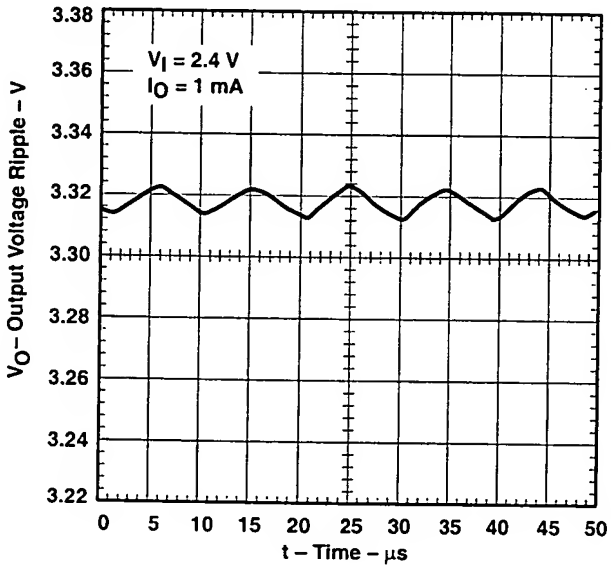


Figure 8

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RIPPLE
vs
TIME

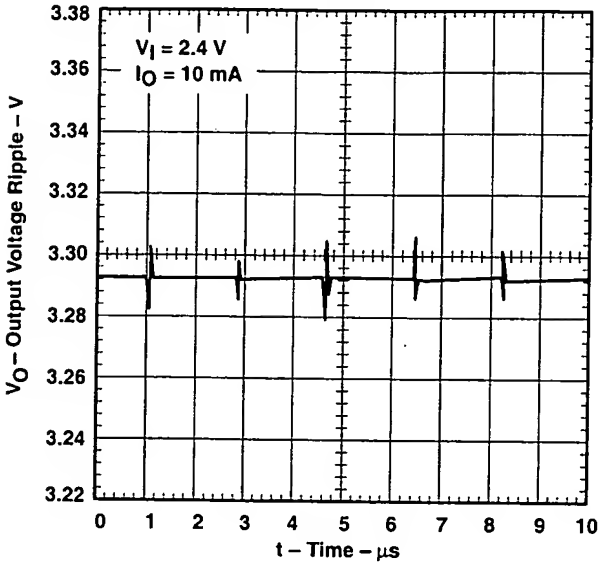


Figure 9

OUTPUT VOLTAGE RIPPLE
vs
TIME

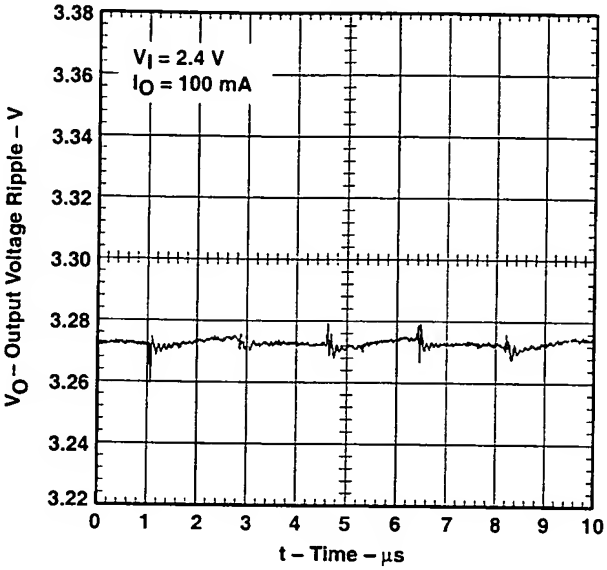


Figure 10

START-UP TIMING

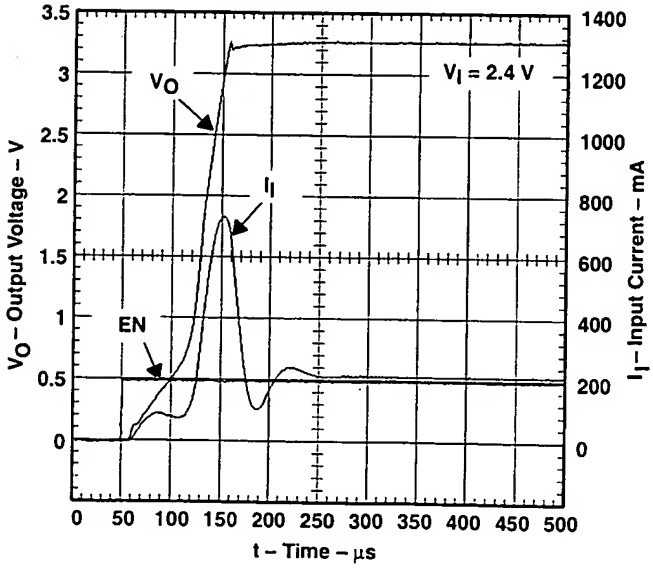


Figure 11

LOAD TRANSIENT RESPONSE

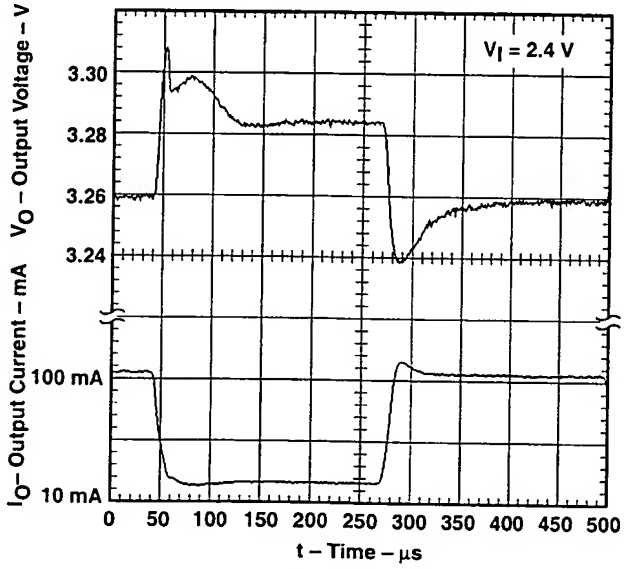


Figure 12

TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

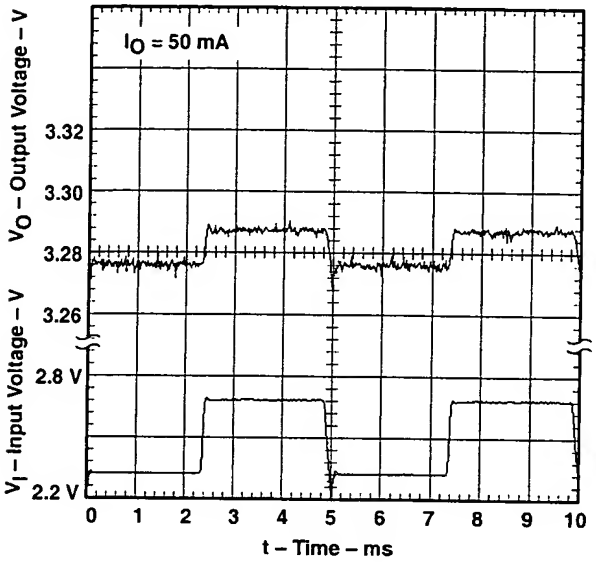


Figure 13

PEAK OUTPUT CURRENT
vs
INPUT VOLTAGE

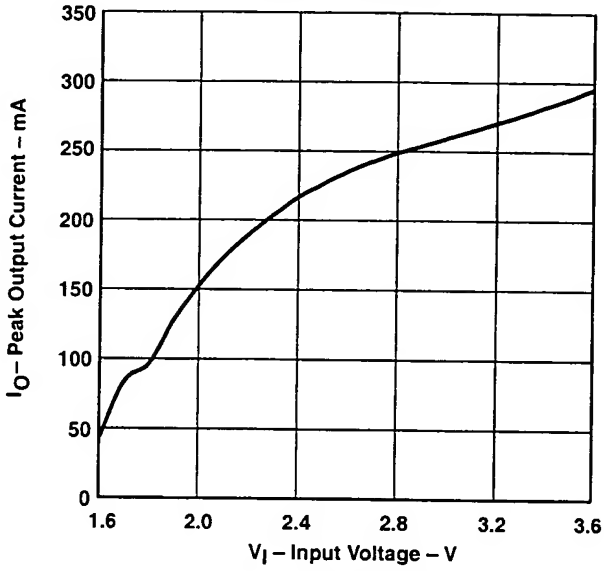


Figure 14

APPLICATION INFORMATION

capacitor selection

The TPS6020x devices require only four external capacitors to achieve a very low output voltage ripple. The capacitor values are closely linked to the required output current. Low ESR (<0.1 Ω) capacitors should be used at input and output. In general, the transfer capacitors (C1 and C2) will be the smallest; a 1-µF value is recommended for maximum load operation. With smaller capacitor values, the maximum possible load current is reduced and the LinSkip threshold is lowered.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from the power source to the converter IC. C_i is recommended to be about two to four times as large as the flying capacitors C1 and C2.

The output capacitor (C_O) should be at minimum the size of the input capacitor. The minimum required capacitance is 2.2 µF. Larger values will improve the load transient performance and will reduce the maximum output ripple voltage.

Only ceramic capacitors are recommended for input, output, and flying capacitors. Depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U- or Y5V-type capacitors will decrease in capacitance. Table 2 lists the recommended capacitor values.

Table 2. Recommended Capacitor Values (Ceramic X5R and X7R)

LOAD CURRENT, I_L (mA)	FLYING CAPACITORS, C1/C2 (µF)	INPUT CAPACITOR, C_i (µF)	OUTPUT CAPACITOR, C_O (µF)	OUTPUT VOLTAGE RIPPLE IN LINEAR MODE, $V_{(P-P)}$ (mV)	OUTPUT VOLTAGE RIPPLE IN SKIP MODE, $V_{(P-P)}$ (mV)
0–100	1	2.2	2.2	3	20
0–100	1	4.7	4.7	3	10
0–100	1	2.2	10	3	7
0–100	2.2	4.7	4.7	3	10
0–50	0.47	2.2	2.2	3	20
0–25	0.22	2.2	2.2	5	15
0–10	0.1	2.2	2.2	5	15

Table 3. Recommended Capacitor Types

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	UMK212BJ104MG	0805	0.1 µF	Ceramic
	EMK212BJ224MG	0805	0.22 µF	Ceramic
	EMK212BJ474MG	0805	0.47 µF	Ceramic
	LMK212BJ105KG	0805	1 µF	Ceramic
	LMK212BJ225MG	0805	2.2 µF	Ceramic
	EMK316BJ225KL	1206	2.2 µF	Ceramic
	LMK316BJ475KL	1206	4.7 µF	Ceramic
	JMK316BJ106ML	1206	10 µF	Ceramic
AVX	0805ZC105KAT2A	0805	1 µF	Ceramic
	1206ZC225KAT2A	1206	2.2 µF	Ceramic

APPLICATION INFORMATION

Table 4. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	http://www.t–yuden.com/
AVX	X7R/X5R ceramic	http://www.avxcorp.com/

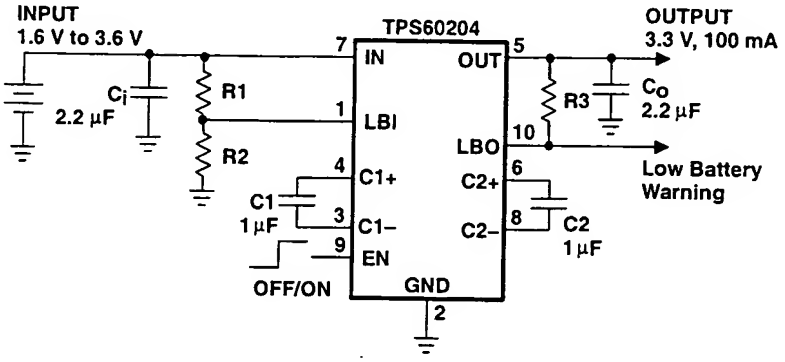


Figure 15. Typical Operating Circuit TPS60204 With Low-Battery Detector

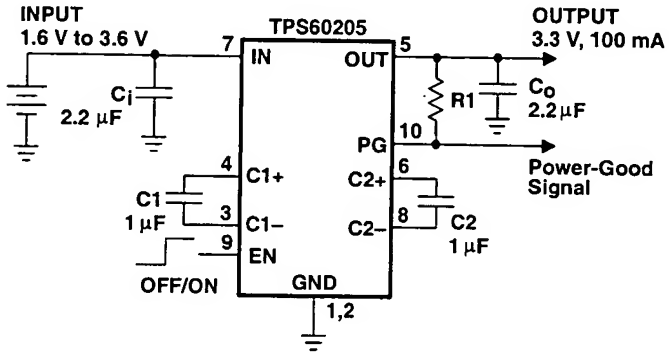


Figure 16. Typical Operating Circuit TPS60205 With Power-Good Detector

APPLICATION INFORMATION

power dissipation

The power dissipated in the TPS6020x devices depends mainly on input voltage and output current and is approximated by:

$$P_{(DISS)} = I_O \times \left(2 \times V_I - V_O\right) \text{ for } I_{(Q)} < I_O \quad (5)$$

By observing equation 5, it can be seen that the power dissipation is worst for highest input voltage V_I and highest output current I_O. For an input voltage of 3.6 V and an output current of 100 mA the calculated power dissipation $P_{(DISS)}$ is 390 mW. This is also the point where the charge pump operates with its lowest efficiency.

With the recommended maximum junction temperature of 125°C and an assumed maximum ambient operating temperature of 85°C, the maximum allowed thermal resistance junction to ambient of the system can be calculated.

$$R_{\Theta JA(max)} = \frac{T_{J(MAX)} - T_A}{P_{DISS(max)}} = \frac{125°C - 85°C}{390\ mW} = 102°C/W \quad (6)$$

P_{DISS} must be less than that allowed by the package rating. The thermal resistance junction to ambient of the used 10-pin MSOP is 294°C/W for an unsoldered package. The thermal resistance junction to ambient with the IC soldered to a printed circuit using a board layout as described in the application information section, the $R_{\Theta JA}$ is typically 200°C/W, which is higher than the maximum value calculated above. However, in a battery powered application, both V_I and T_A will typically be lower than the worst case ratings used in equation 6 , and power dissipation should not be a problem in most applications.

layout and board space

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be placed in close proximity to the device. A PCB layout proposal for a one-layer board is given in Figure 17. There is no specific EVM available for the TPS60204. However, the TPS60200EVM–145 can be used to evaluate the device.

The evaluation module for the TPS60200 can be ordered under product code TPS60200EVM–145. The EVM uses the layout shown in Figure 17. All components including the pins are shown. The EVM is built so that it can be connected to a 14-pin dual inline socket, therefore, the space needed for the IC, the external parts, and eight pins is 17,9 mm x 10,2 mm = 182,6 mm^2.

APPLICATION INFORMATION

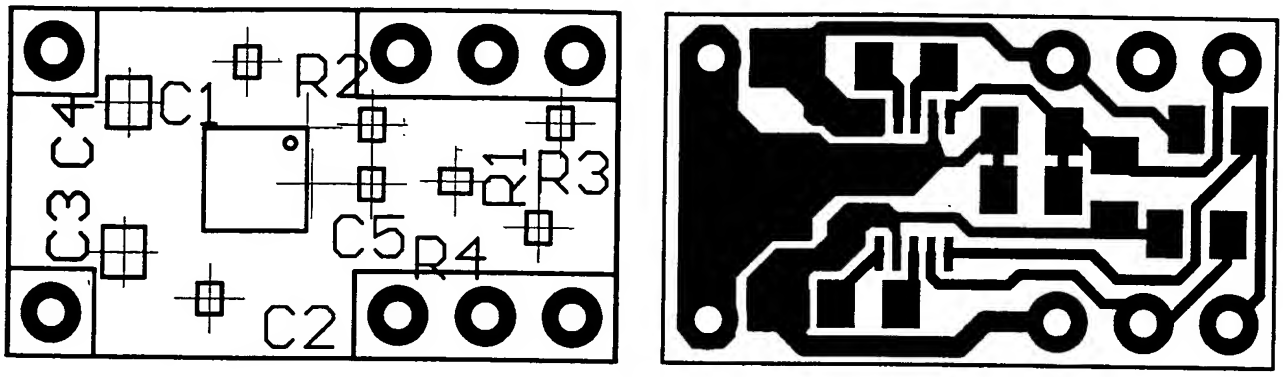


Figure 17. Recommended Component Placement and Board Layout

Table 5. Component Identification

IC1	TPS60204
C1, C2	Flying capacitors
C3	Input capacitors
C4	Output capacitors
C5	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO
R4	Pullup resistor for EN

Capacitor C5 should be included if large line transients are expected. This capacitor suppresses toggling of the LBO due to these line changes.

device family products

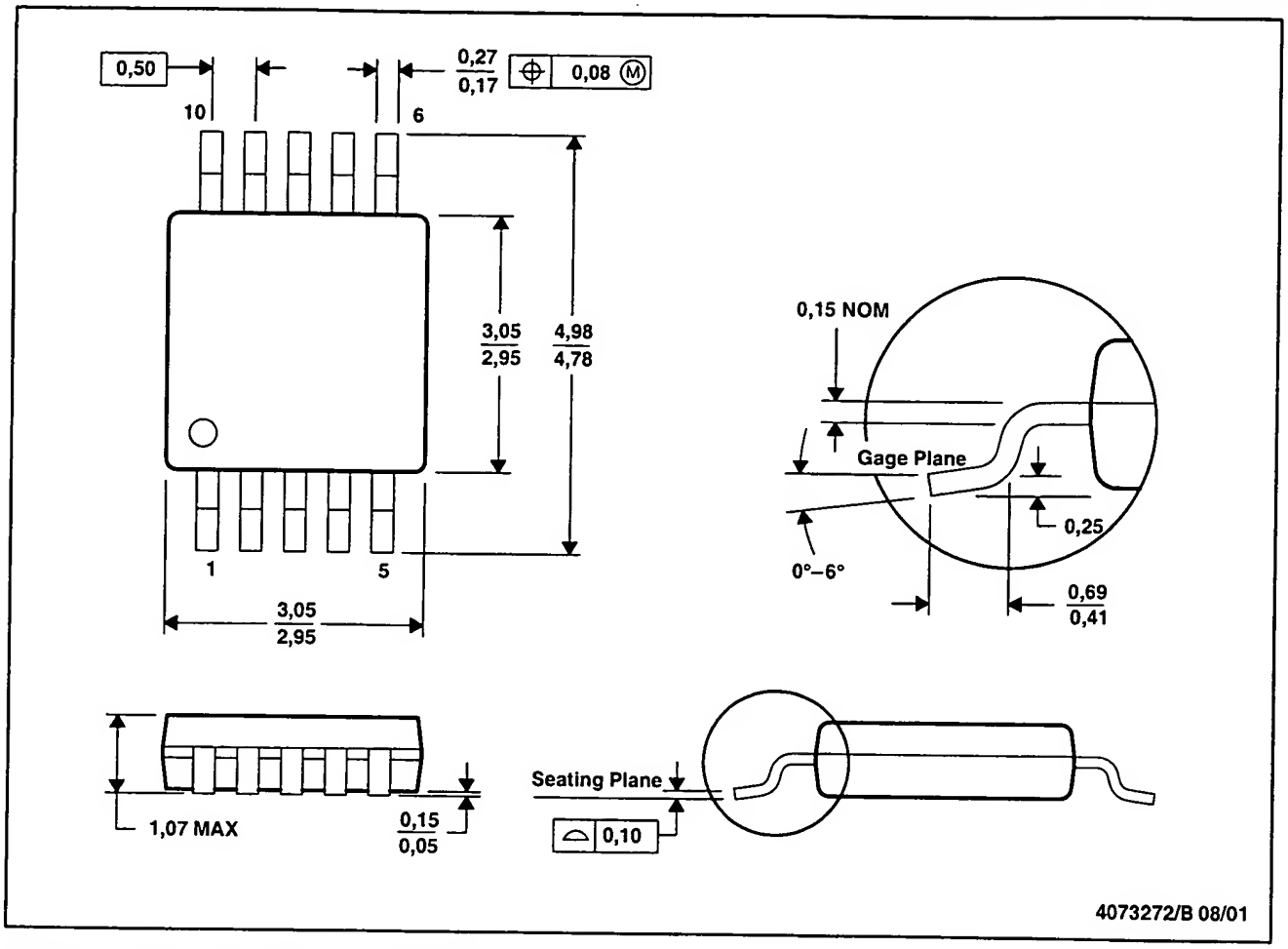
Other charge pump dc-dc converters in this family are:

Table 6. Product Identification

PART NUMBER	DESCRIPTION
TPS60100	2-cell to regulated 3.3 V, 200-mA low-noise charge pump
TPS60101	2-cell to regulated 3.3 V, 100-mA low-noise charge pump
TPS60110	3-cell to regulated 5.0 V, 300-mA low-noise charge pump
TPS60111	3-cell to regulated 5.0 V, 150-mA low-noise charge pump
TPS60120	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with low battery comparator
TPS60121	2-cell to regulated 3.3 V, 200-mA high efficiency charge pump with power-good comparator
TPS60122	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with low battery comparator
TPS60123	2-cell to regulated 3.3 V, 100-mA high efficiency charge pump with power-good comparator
TPS60130	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with low battery comparator
TPS60131	3-cell to regulated 5.0 V, 300-mA high efficiency charge pump with power-good comparator
TPS60132	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with low battery comparator
TPS60133	3-cell to regulated 5.0 V, 150-mA high efficiency charge pump with power-good comparator
TPS60140	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with low battery comparator
TPS60141	2-cell to regulated 5.0 V, 100-mA charge pump voltage tripler with power-good comparator

MECHANICAL DATA

DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

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LINEAR TECHNOLOGY

DESIGN NOTES

New Charge Pumps Offer Low Input and Output Noise

Design Note 243

Sam Nork

Charge pump (inductorless) DC/DC converters are quite popular in space-constrained applications where low to moderate load currents must be supplied. Such converters are available in small packages, operate with very low quiescent current and require minimal external components. However, noise generation is one undesirable characteristic of most charge pumps.

Unwanted noise can create a variety of problems. Noise generated at the power input can interfere with RF transmission and reception in wireless applicatons. Noise at the output can couple onto sensitive circuits or even create audible noise. The new LTC®3200 family of boost charge pumps employs a new architecture designed to minimize noise at the input and output to mitigate such unwanted behavior.

Burst Mode™ Operation vs Constant Frequency

Most regulating charge pump DC/DC converters operate using a Burst Mode architecture. Such regulator architectures provide the lowest quiescent current, but generate the highest levels of both input and output noise. With Burst Mode parts, the charge pump switches are either delivering maximum current to the output or are turned off completely. A hysteretic comparator and reference control the turn-on and -off of the charge pump to provide output regulation. Low frequency ripple appears at the output and is required for regulation (see Figure 1). This bursting on and off also results in large input ripple current that must be supplied by the input source. Any impedance in the input source creates voltage noise at the input. This noise must then be rejected by the rest of the circuitry powered from the same source.

The LTC3200 and LTC3200-5 have been designed to minimize both input and output noise. These parts are regulating boost charge pumps that can supply up to 100mA of output current. The LTC3200-5 produces a regulated 5V output and is available in a 6-lead SOT-23 package. The LTC3200 produces an adjustable output voltage and is available in an 8-lead MSOP package. Both parts use a constant-frequency architecture that eliminates low frequency output noise. Charge pump switching is continuous, even with no load, and a linear control loop regulates the amount of charge transferred to the output on each clock cycle. Since the output regulation loop is linear, the peak-to-peak output ripple can be approximated as $V_{RIPPLE} = (I_{LOAD}/C_{OUT})/(2 \cdot f_{OSC})$, with no additional ripple due to regulator hysteresis.

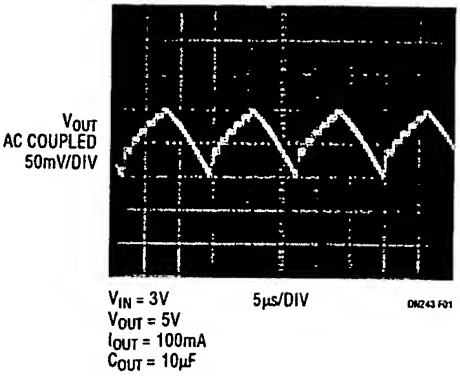

Figure 1. Typical Burst Mode Output Ripple

The parts' 2MHz oscillator frequency allows low output ripple to be achieved even with small output capacitors. Figure 2 illustrates the output ripple achievable with the LTC3200-5 supporting a 100mA load with different values of output capacitance.

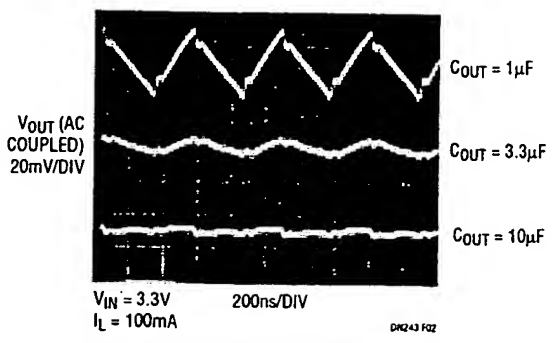

Figure 2. LTC3200-5 Output Ripple

Input Noise Reduction

Although constant frequency generation alone provides substantial input noise improvement, the LTC3200 family goes one step further. A unique internal control circuit regulates the input current on both phases of the charge pump clock. This technique prevents RC current decay during one or both half-clock cycles of the charge pump oscillator, thereby minimizing the input-referred ripple due to changing input current. Figure 3 shows the difference in input noise between the LTC3200 and a typical Burst Mode charge pump. Both parts are shown producing a regulated 5V output at 100mA of output current from a 3.6V input. 0.1Ω of input impedance is used for testing purposes. The typical Burst Mode part uses 10µF ceramic capacitors at both the input and the output. The LTC3200 uses 1µF ceramic caps of the same dielectric. As shown in Figure 3, significant improvements in input noise are achieved with the LTC3200—even with one-tenth the bypass capacitance.

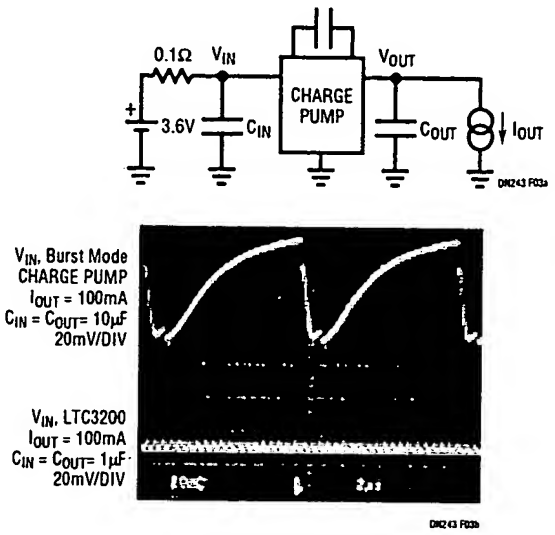

Figure 3. Input Noise Test Circuit

Typical Applications

Charge pumps are commonly used to provide low power boost conversion inside handheld devices such as cellular phones and PDAs. Such devices, particularly those which contain RF communication, tend to be very sensitive to noise. A popular application for a low noise charge pump in such products is powering white LEDs used for backlighting a small color LCD display. The circuit shown in Figure 4 produces a low noise boosted supply for driving up to six white LEDs. The LTC3200's FB pin is used to regulate the LED current flowing through each ballasted LED. By using the LTC3200, the user can provide boosted power to the backlight circuit directly from the battery without the cumbersome problem of filtering low frequency noise.

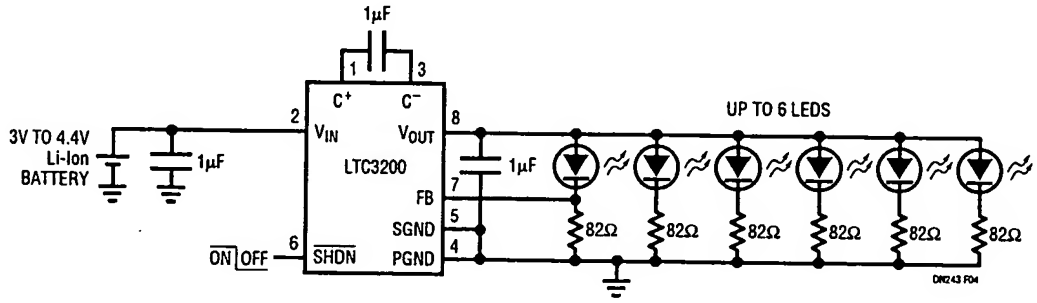

Figure 4. Low Noise White LED Driver with LED Current Control

Data Sheet Download

http://www.linear-tech.com/go/dnLTC3200

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Press Releases -- Dec 1998

LTC1550L/LTC1551L: Low Noise Charge Pump Inverters in MS8 Shrink Cell Phone Designs

MILPITAS, CA— December 4, 1998 — Linear Technology introduces the LTC1550L and LTC1551L, low-noise switched capacitor regulated voltage inverters for saving space in cell phones and similar applications. Designed for biasing GaAs FETs, both parts come in the compact 8-pin MSOP package and can operate from a single Li-Ion battery. Their 900kHz charge pump with a linear post regulator provides clean output with small components. This makes the LTC1550L and LTC1551L ideal for compact cell phone designs and in mobile radio and wireless modems and wireless LANs that need a well-regulated, low-noise negative bias supply. The LTC1550L and LTC1551L operate from a supply voltage (V_{CC}) of 2.7V to 5.5V and deliver an output voltage adjustable from -1.3V to -5.25V. Output current from a V_{CC} of 3.5V is 20mA at $-1.5V_{OUT}$ and up to 5mA at $-3.0V_{OUT}$. Output voltage regulation is ±2.5% and output ripple is less than $1mV_{P-P}$. Both parts also include a REG function to sense when output voltage is within 5% of a set value, which helps protect GaAs FETs that require a valid negative bias voltage at their gate before voltage is applied to the drain. The LTC1550L includes an active low Shutdown pin (SHDN) while the LTC1551L's Shutdown pin is active high. Both parts are available in fixed and adjustable output versions housed in 8-lead SO and MSOP packages; prices start at $1.70 per part per 1,000 pieces. The LTC1550L is also available in an adjustable 16-lead SSOP version priced at $1.90 per part per 1,000 pieces. All versions are available immediately from stock.

Summary of Features:

LTC1550L/LTC1551L Low Noise Charge Pumps

- Regulated negative voltage from a single positive supply
- Low output ripple: Less than 1mVP-P
- Output voltage regulation: ±2.5% over line, load and temperature
- Fixed -2V, -2.5V and –4.1V output or adjustable output (-1.5V to -4.5V)
- REG pin indicates when output voltage is within 5% of its regulated negative voltage
- Small charge pump capacitors (0.1μF)
- 900kHz charge pump frequency
- Requires only four external capacitors
- Shutdown mode drops supply current to <1μA
- High output current: Up to 20mA

Back to top

Accurate Phase Noise Prediction in PLL Synthesizers

Part 2: Here is a method that uses more complete modeling for wireless applications

By Lance Lascari
Adaptive Broadband Corporation

As discussed in part one of this article, published in the April issue of *Applied Microwave & Wireless*, phase noise characteristics of the frequency synthesizer contribute greatly to system performance. In this concluding section, we will show and discuss experimental results for the op-amp in loop filter.

Design goals	Value	Comments
Output Frequency	865 MHz	
Reference Frequency	200 kHz	
Frequency Step Size	12.5 kHz	
PLL Loop bandwidth	750 Hz	Get as close as possible with available components
Phase Margin	55 degrees	
Additional Reference Frequency Attenuation Required from the Third Pole	10 dB	

▲ **Table 2. Design goals for the example loop filter design.**

Op-amp in loop filter

While the cases using the passive loop filter (no op-amp) are simply a matter of circuit analysis, the case using the active filter requires some explanation. This case will only be described here; the accompanying analysis can be found in the supporting MathCad documents.

With the op-amp in the loop, and the filter configuration shown in Figure 1, four different noise sources and important factors exist within the loop itself: R_2, the op amp itself, the gain of the op-amp, and R_3.

The noise within R_2 is the same as the cases previously mentioned. However once this noise is determined, the gain of the amplifier needs to be applied to it (amp_gain in Figure 1). The output of the op-amp is again filtered by R_3 and C_3. A schematic of this is pictured in Figure 2a.

The op-amp itself contributes noise, and this is one reason to place the op-amp after the second order filter section but before the third pole. The third pole can then provide some attenuation of the broadband noise. Manufacturer's data sheets will usually specify the input noise of the op-amp in $nV/\sqrt{Hz}$. This noise voltage is simply multiplied by the amplifier's gain (amp_gain), and then passed through the filter formed by R_3 and C_3.

Op-amps are usually regarded as very low-output-impedance devices. For this reason, the analysis of the noise due to R_3 can be greatly simplified if an op-amp is in the loop as shown in Figure 1. If it is assumed that the op-amp output impedance is virtually a short (which would be accurate, even if the op-amp output were a few hundred ohms), then the noise voltage generated in R_3 is simply connected to ground, then filtered through R_3 and C_3.

Practical design example

To show the effect of the resistor noise, two different loop filters were designed to meet the basic specifications outlined in the goals section of Table 2. The only differences between the filters were their implementation of the third

pole. The values used in each of the designs were typical of what one designer might choose over another.

Experimental setup

Equipment used in the lab setup included a Hewlett-Packard 8563E spectrum analyzer with the phase noise utility software (P/N HP85671A) installed; a PC running a custom application developed to gather tabular data after the phase noise utility was run; and the PLL synthesizer under test (modified standard product produced by Adaptive Broadband Corporation).

The results presented in Figures 9 and 10 represent five averages of each phase noise measurement. In order to show the limitations of the measuring system, (i.e. the spectrum analyzer), the phase noise of the extremely low noise HP 8642B signal generator was plotted for comparison purposes. At higher offset frequencies where the measurements and models begin to disagree, it is clear that that the noise floor of the spectrum analyzer is contributing to measurement error.

Component/Specification	Value	Comments
Synthesizer IC, National LMX2350 Fractional-N PLL	Allows 1/16th Fractional mode	
Phase Detector Noise Floor (Npd_ref from Equation 6)	–200 dBc/Hz	Data supplied by National Semiconductor.
Phase Detector Gain	1.6 mA/cycle	Set to maximum for this design.
VCO Tuning Sensitivity, K_{vco}	27 MHz/volt	Custom vendor supplied component, measured at frequency of interest.
VCO Phase Noise	–103 dBc/Hz at 10 kHz offset	Measured for this particular device using a very narrow and quiet loop.
TCXO reference oscillator Frequency	12 MHz	
TCXO reference oscillator Phase Noise (Ntxco_ref from Equation 7)	–125 dBc/Hz at 100 Hz offset	This number was estimated from measurement data from many PLLs. This is roughly 10 dB worse than published data on a similar product from the TCXO vendor. Measurements for the model used were unavailable.

▲ **Table 3. Specifications for the components available.**

Loop Filter Component Values	Value for Case 1	Value for Case 2
C1	0.1 μF	0.1 μF
R2	500 ohms	500 ohms
C2	1 μF	1 μF
R3	1 kohm	10 kohm
C3	1000 pF	100 pF

▲ **Table 4. Component values for the two loop filters studied.**

Discussion of experimental results

Figures 9 and 10 show excellent agreement between the modeled phase noise of the synthesizers and the measured results. The conclusion that must be drawn is resistor noise can be a very significant contributor to synthesizer phase noise, and thus needs to be considered in all low-noise synthesizer designs. For the case of these experiments, and others performed by the author, the models presented accurately predict this noise, allowing the analysis of all of these degradations at the time the loop is designed [1].

The loop filters for case 1 and case 2 both meet the basic requirements of the design but have drastically different phase noise characteristics. For instance, at the 10 kHz offset points, the two synthesizers differ in phase noise by almost 10 dB. For narrowband systems with channels spaced at this interval, this would equate to a difference in adjacent channel rejection of 10 dB when comparing case 1 to case 2. Although the resistors are much smaller in the case 1 analysis, the noise contribution should not be ignored.

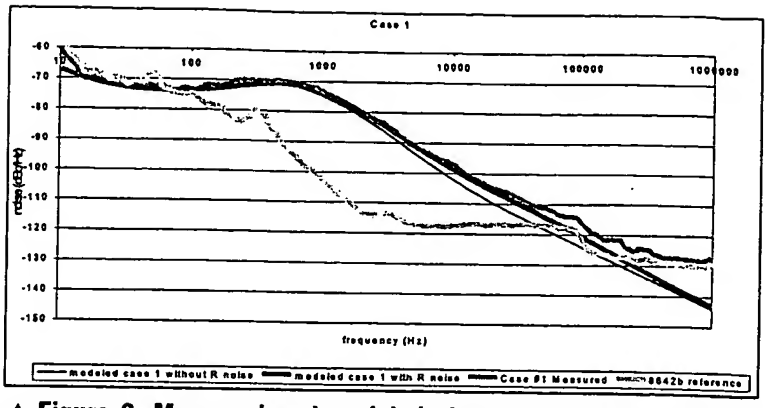
Even more significant than the agreement well outside of the loop bandwidth is the agreement near the loop bandwidth. Since the magnitude of the noise that falls near the loop corner is much larger than the noise far outside of the loop bandwidth, it contributes significantly to the RMS phase error and residual FM metrics. These metrics are very indicative of the performance degradations caused by frequency synthesizers in QAM and FM/FSK systems respectively. If the synthesizer noise were modeled without resistor noise, the results would be dramatically different, especially for case 2.

Reducing resistor and op-amp noise contributions

When designing a frequency synthesizer, there are

often several degrees of freedom that can be exercised in order to minimize the system phase noise. If there are no degrees of freedom, up-front design analysis will at least show an accurate prediction of the phase noise. This prediction may help to make system tradeoffs rather than sticking to a more stringent synthesizer specification.

In most synthesizer designs, it seems that R3 is typically the single most significant contributor to the resistor noise. This begs the question, "Is the third pole really needed?" If the reference suppression within the loop is sufficient without the third pole, it is in the designer's best interests to leave these parts out of the design. If this pole is required, the value of R_3 should be kept as small as possible without upsetting the basic filter response.



▲ **Figure 9. Measured and modeled phase noise of the example synthesizer, case 1.**

Some VCO designs themselves use resistors to supply the tuning voltage to the varactor (the similarity to the R_3 analysis is staggering). In many published VCO designs, large resistors are used to feed the varactor. This is a good choice for simple, and low-cost designs since resistors are inexpensive, resonance-free, and they don't typically degrade resonator Q if they're large relative to the other shunt resistances in the circuit. Resistors are hardly a good choice, however, if the tuning sensitivity (VCO gain) is high. The noise contribution by this resistor is proportional to its value alone in this case; a small resistor in series with a choke may be a good choice in many applications.

Op-amps, even if chosen carefully, represent significant contributions to phase noise. The synthesizer designer should be careful to determine whether an op-amp is truly required in order to meet the system requirements. If increased voltage is required, consider using an external charge pump with higher supply voltages (some synthesizer ICs still support the connections required for using an external charge pump). Obtaining good balance in an external charge pump can be difficult, leading to increased reference spurs and power supply noise at the reference frequency. A low noise charge pump potentially offers reduced noise over the op-amp, as the tuning voltage range can be increased with a designer-chosen charge pump current. This represents two degrees of freedom: lower tuning sensitivity and reduced resistor values due to potentially increased current. It would be excellent if the available synthesizer chips allowed for higher tuning voltages or specifically allowed for simple implementations of well-balanced external charge pumps.

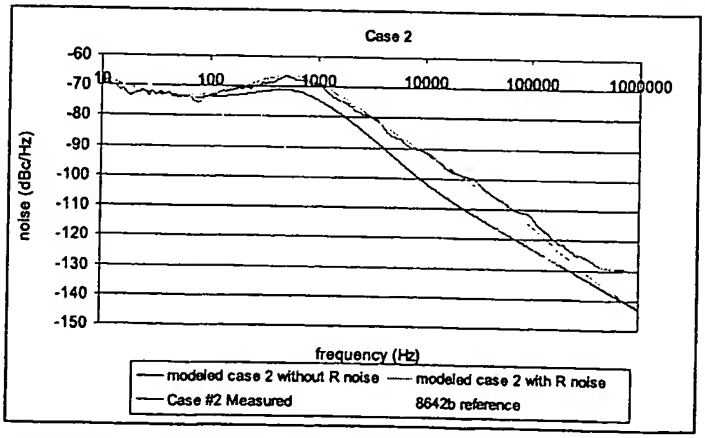
Reducing the VCO tuning sensitivity is another way to reduce the overall noise. This needs to be analyzed on a case-by-case basis, however, since the loop filter resistor values will increase with reduced tuning sensitivity. Any fixed magnitude noise sources in the loop will also drop proportionally with the VCO tuning sensitivity.

One particular option the author feels worthy of exploration is increasing charge pump current. With increased charge-pump current, the impedance (hence resistance) in the loop drops. If your synthesizer has a programmable charge pump current setting, leaving it at maximum is best in order to reduce the resistor noise contribution.

Each of the suggestions presented carries with it some design implication that needs to be carefully evaluated before tradeoffs are made. In some designs, simply increasing charge-pump current or eliminating the 3rd pole used for reference attenuation could yield dramatic improvement.

Conclusion

In order for designs to meet the increasingly demanding performance requirements in the wireless arena, a detailed understanding of every component is critical. While relatively simple, the models presented have demonstrated excellent accuracy when compared to experimental data. These circuit models represent new tools that enable the designer to make important tradeoffs during the initial synthesizer design phase, rather than on the bench using empirical and time-consuming techniques. ■



▲ **Figure 10. Measured and modeled phase noise of the example synthesizer, case 2.**

Acknowledgements

I would like to thank John Barenys of Adaptive Broadband for writing the phase noise curve acquisition program for the PC, which were invaluable in the preparation of this article. Thanks also to Dean Banerjee of National Semiconductor for providing many insightful email discussions and critiques of the work presented here. The support of Adaptive Broadband and numerous discussions with my fellow employees were very valuable during the preparation of this work. I also appreciate the efforts of the many people who helped by reviewing this article.

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